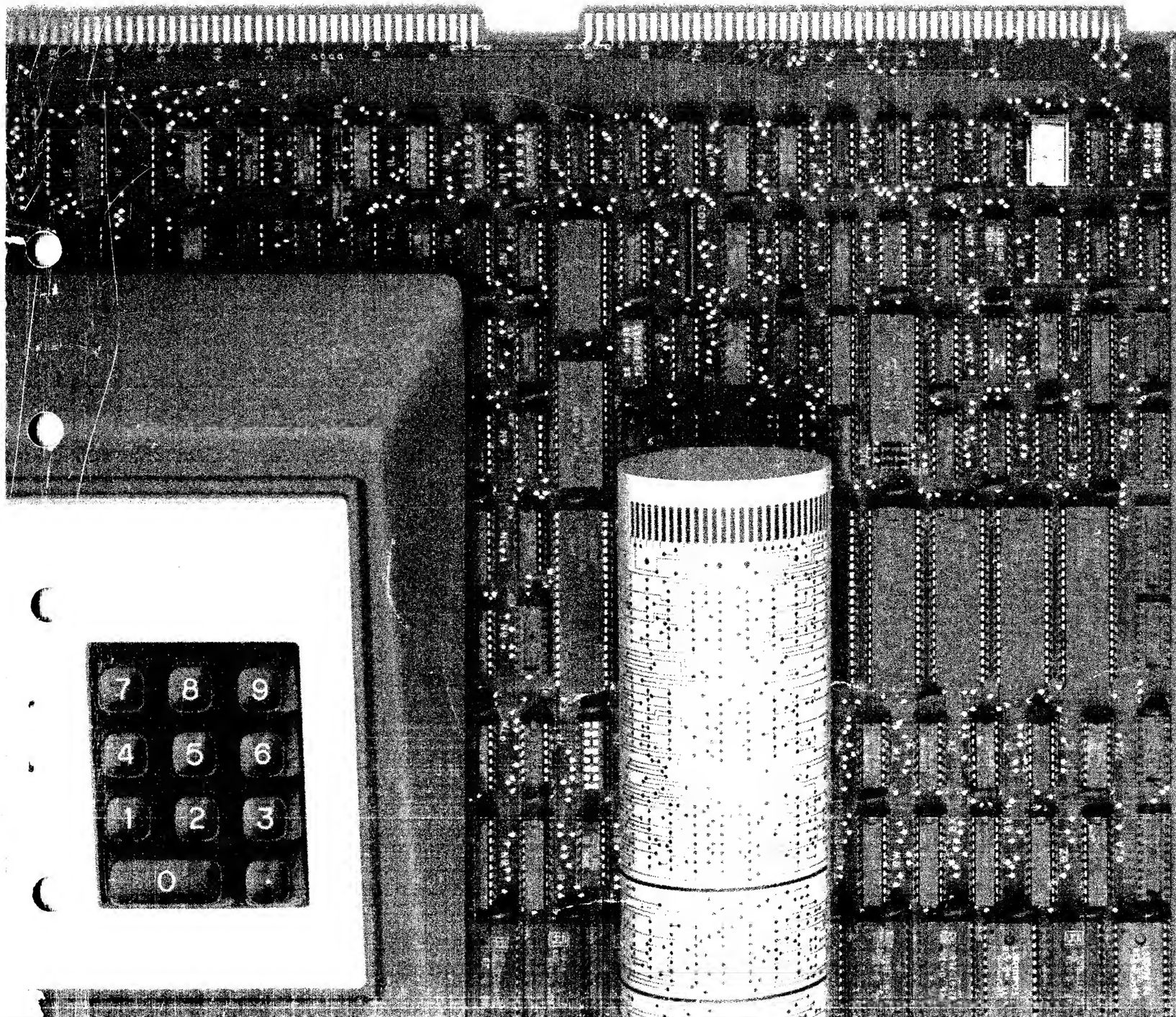
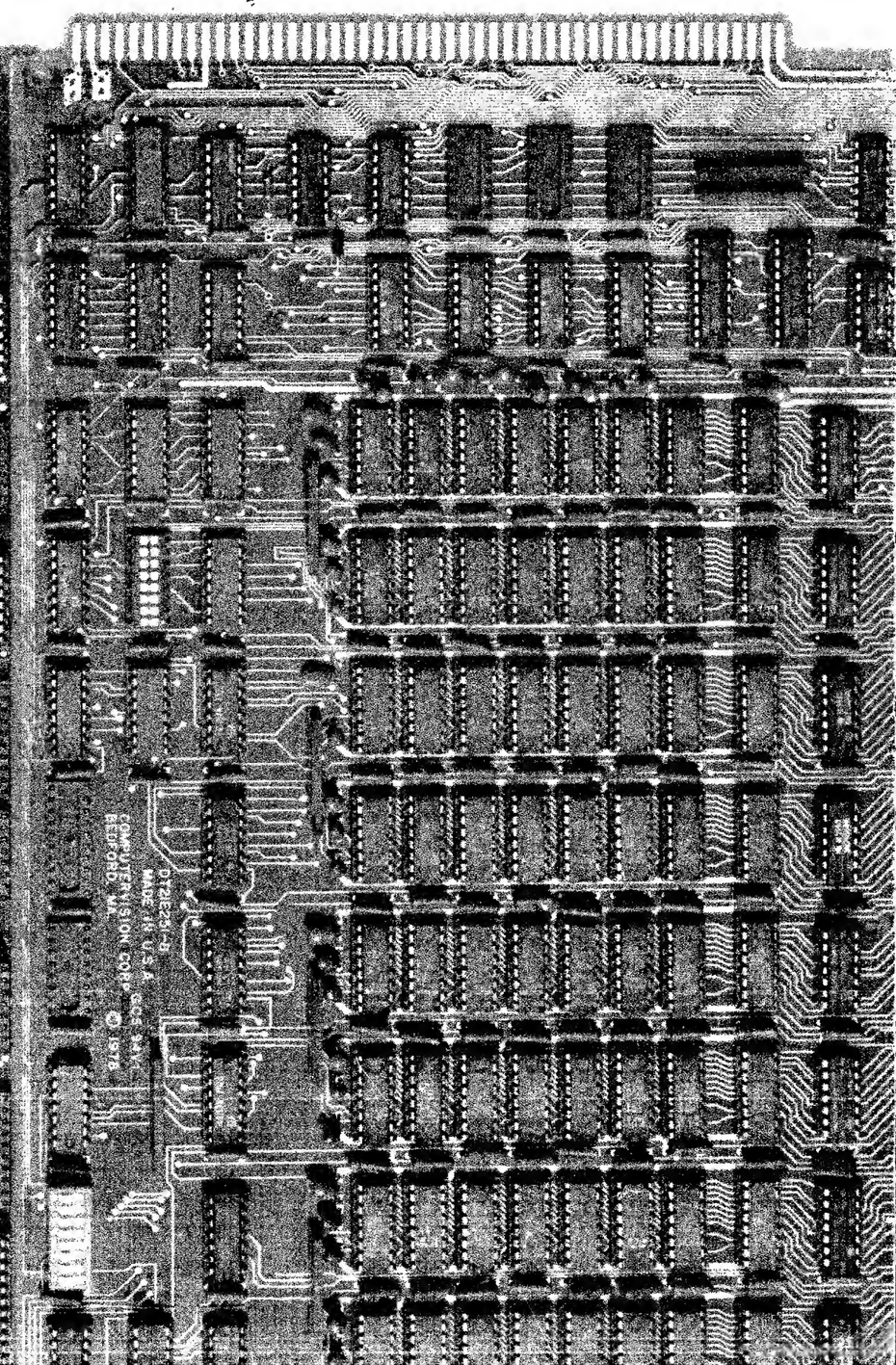
COMPUTERVISION

Technical

Graphics Processing Unit (GPU)

Logic Diagrams





Document control number: 32- 00376

Name: _____

Graphics Processing Unit

Logic Diagrams

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NOTES
1. ⟶ CONTROL STORE BIT(S).
2. ⟶ PIO COMMAND.
3. Ø IS MSB.
4. ( ) = SCHEMATIC PAGE NO.

FARERR
PPULSE
OROUTFIF
FBYT3=Ø
FBYT2=Ø
F=Ø
OVR1
F3
FLGCTRL(Ø:1)
TADR(Ø:3)
LDCOND
ANYENT
IMØ
IBØ
F=Ø
F3
IBØ:7
IB8:15
TEST BYTE 1 16X8 (15)
TEST BYTE 2 16X8 (15)
TADR (Ø:3)
IBDST(2)
FLAGS (15)
LATCHED CONDITIONS (15)
DYN COND (15)
TBØ:7
TB 3:7
TSTBYT(Ø:2)
BA(8:11)
TB4:7
DECODE FPLA (16)
MULTI WAY BRANCH ROM 256x4 (16)
TSTBIT(Ø:2)
INV
CC
BA (4:7)
BA Ø:1
BI (Ø:3)
BA (Ø:3)
BI (Ø:4)
MICRO SEQUENCER 2910 (16)
PAGE
RAØ:11
IBSRC(Ø:3) =8
IB4:15
IB3
IBUSØ:23

CONTROL STORE
3KORGK X88
(17, 18, 19)

IBDST(7:1Ø)= DECODE
Ø IBTOBMAR
1 IBTOBMEM
2 IBTOCAR
3 IBTOOUTFIF
4 INSTEND
5 TASKTERM
6 DIVIDE
7 MULGO
8 IMTOMUL1
9 IMTOMUL2
10 IMTOMUL3
11 IMTOMUL4
12 ANYENT

IBSRC(Ø:3)= DECODE
Ø SHF1TOIB
1 SHF2TOIB
2 SHF3TOIB
3 SHF4TOIB
4 INFIFTOIB
5 IMEMTOIB
6 ROMTOIB
7 ALUTOIB
8 RATOIB
9 IMARTOIB

IBDST(BIT) DEST
(Ø) IBTOIMAR
(1) IBTOIMEM
(2) IBTOTEST
(3) IBTOSHF1
(4) IBTOSHF2
(5) IBTOSHF3
(6) IBTOSHF4

IBUS BYTE#
RDSEL= 1 2 3
Ø 1 2 3
1 1 1 1
2 2 2 2
3 3 3 3
SOURCE BYTE#

WRTSEL BITS
35 SET→WRITE BYTE 1
36 SET→WRITE BYTE 2
37 SET→WRITE BYTE 3

INV
XCYC
BSEL
SEL6
INCIMAR

FLGCTRL=
Ø ILLEGAL
1 CLRFLAGS
2 LDFLAGS
3 NOP
LDCOND

TSTBYT= SELECT
Ø TSTBYTE 1
1 TSTBYTE 2
2 FLAGS
3 LAT. COND
4 DYN. COND
TSTBIT
PAGE

A | B | ALU | CN | SADR | MADR | TADR | BI | BA
Ø 3|4 7|8 16|17 18 21|22 32|33 35 37|38 41|42 51|52|53|54|55|56|57 59|60 63|64 66|67 69|70 74|75|76 87

IB 12:15
XTAL (4)
÷ 2
(TO MULT) 18 MHZ
9 MHZ
SEQ CTRL MODE LOGIC ROM 256X4 (2)
DOC
=5
TASKTERM
INSTEND
=4
FROM IBDST (7:1Ø)
COMPLETE
6 WAIT CONDITIONS
IBSRC(Ø:3)
IBDST(7:1Ø)
WAIT LOGIC (4)
WAIT
BUSY
XCYC
CLOCK CTRL LOGIC & ROM 32X8 (4)
GPUCLK

IBDST(1)
DIB
DOB
DIB
DRIVER (3)
OUT FIFO (3)
DATAØ:15
IBØ:15
IBDST (7:1Ø)
DIA
PIO XCVR (2)
DATAØ:15
IEØ:15
I/O DATA BUS Ø:15 & CONTROL

START
CLR
IORST
IOPLS
SELB
SELD
INTR
I/O LOGIC (1)
BUSY
DONE
DRIVER (1)
DATAIØ:15
JUMPER DEVICE SELECT
INTA

IB2:23
WRITE DRIVER (6)
FROM FPLA
BMADØ:2
BMCØ:3
BMEMBUSØ:15
CAR (5)
READ XCVR (5)
IBDST(7:1Ø)
=2
IN FIFO (5)
IBSRC(Ø:3)
=4
IBØ:15
TO WRITE DRIVER
TO READ XCVR
FROM FPLA
BPORT
BMADØ:2
BMCØ:3
BMEMBUSØ:15
& CONTROL

BUSY
=Ø
=1
=2
IBDST(7:1Ø)
BMEM CTRL LOGIC & FPLA (4)
CLKIN
BLDMAR
BMEMRD
BMEMWRT
BMEMBSY
DIFF DRIVER (4)

DS23E017
C

BLOCK DIAGRAM

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TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 1°00'

MATERIAL
FINISH

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
C	ECO #3241			
B	ECO 3102	RB		
A	REL ECO 3075			
1	ISSUE			

DRN T. Wilson 9/1/82
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

PART NUMBER	NEXT ASSEMBLY	QTY
DA23E015	1	

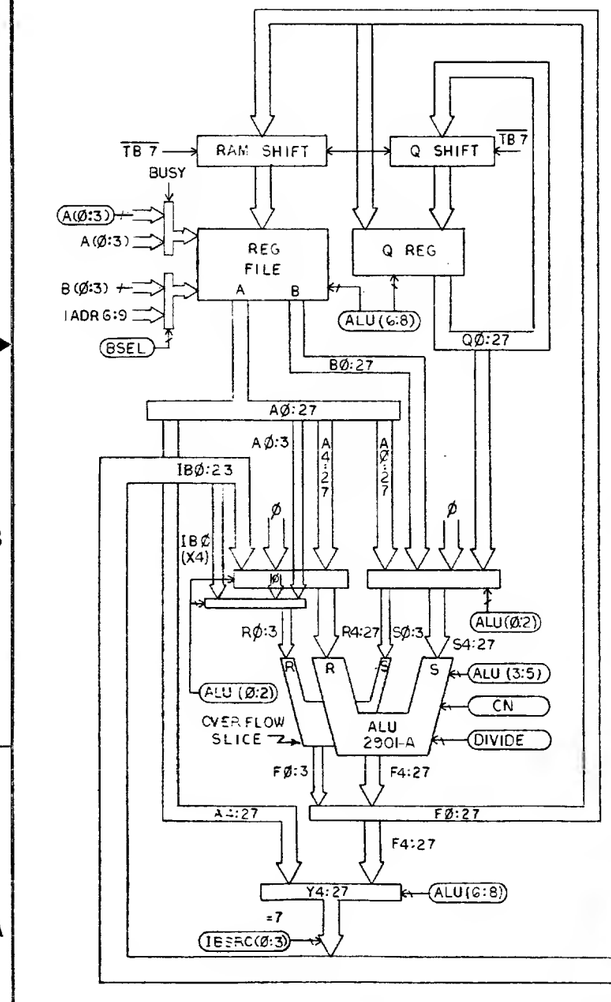
TITLE: GPU SCHEMATIC DIAGRAM

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

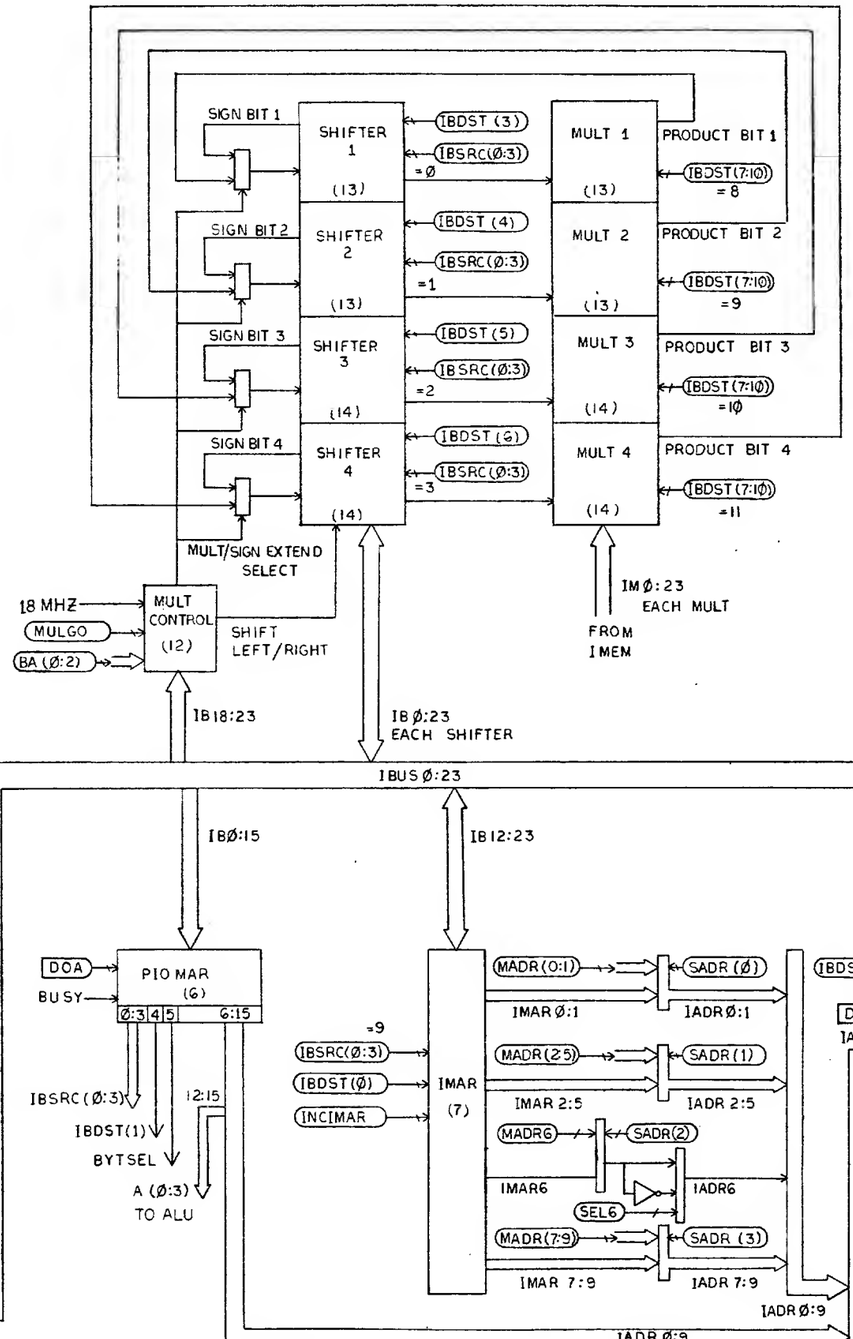
REMOVE ALL BURRS AND SHARP EDGES

SCALE NONE
DWG NO. DS23E017
UNIT WT.
SHEET 1A OF 19 SHEETS

MAKEPEACE P-2059



ENTIRE ALU (10,11)



DS23E017 C

BLOCK DIAGRAM

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TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL
FINISH
DRN
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES
PART NUMBER NEXT ASSEMBLY QTY

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE NONE DWG NO. DS23E017

UNIT WT.

SHEET 2A OF 19 SHEETS

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MAKEPEACE P-2059

GPU SELECT, BUSY, DONE, AND I/O COMMANDS

MSB
LSB
PA 72 DS0/L
PA 88 DS1/L
PA 88 DS2/L
PA 48 DS3/L
PA 82 DS4/L
PA 84 DS5/L
8160 4C
JUMPER 5C
470 R2
+5V
1K R100
8241 3C
DATA10/L
DATA11/L
DATA12/L
DATA13/L
DATA14/L
DATA15/L
PA 52 STRT/P
9MHZ/H
1P FILT
LS11 1R
START
LS74A 1S
74S74 2L
START SYNC
LS08 1L
LS04 1J
RESET-PARERR PE 42
BUSY/H
CIOR/L
7438 1K
SELB/L PA 82
COMPLETE/N
S74A 2L
BUSY
BUSY/L
PA 50 CLR/P
1P FILT
LS10 2N
CLRUADR/L
PA 70 IORST/P
1N FILT
LS00 2M
LS08 1L
LS08 3P
S74A 3L
DONE
SELD/L PA 80
PB 41 RQENB/L
1N FILT
LS08 1M
INTR/L PB 29
INT DIS
LS74A 2K
INT REQ
PA 38 MSKO/L
DATA2/L
S23E017 C
PPULSE/H
PA 74 IOPLS/P
1P FILT
LS11 1R
IOPLS
IORST/N
PA 40 INTA/H
1N FILT
LS08 1M
LS10 3K
LS04 8H
PA 96 INTPIN/L
LS04 1J
7438 1K
330 R6
390 R5
INTPOUT/L PA 95
GPUINTREQ/L
GPUINTREQ/H
1K R103 P/1
1K R1 P/2
1K R14 P/3
1K R3 P/4
1K R16 P/5
1K R17 P/6
1K R18 P/7
1K R15 P/8
1K R100 P/9
1K R103 P/10
1K R100 P/11
1K R100 P/12
1K R4 P/13

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MATERIAL			
FINISH	L23X004	1	DRN S HOSSE
	A23E015	REF	CHK
			ENGR
			PROJ
PART NUMBER	NEXT ASSEMBLY	QTY	MFG

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0050 FRACTIONAL ±1/64 ANGULAR ±.30

SIGNATURE DATE

REMOVE ALL BURRS AND BREAK EDGES

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE DWG NO. S23E017

UNIT WT. SHT 1 OF 19 SHTS

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

IB (0:15)

SEQUENCE CONTROL ROM

IB12
IB13
IB14
IB15
LS175
5K
CLR
LDSCM/N
S301-1
4K
LS32
COMPLETE/N
IORST/N
TASKTERM/L
INSTEND/L
GPUCLK1
SELECT/H
BUSY/L
LS08
1M
PA 58 DATOA/H
LS10
1N FILT
2N
LDPIOMAR/N
PA 56 DATOB/H
PIOWRT/N
PA 46 DATOC/H
1P FILT
2P
LS00
2M
PA 44 DATIA/H
PIORD/N
PA 42 DATIB/H
S10
LS04
4T
PIORDOUTFIF/P

DATA (0:15)/L

PIO XCVR

MSB

PB 62 DATA0/L
PB 85 DATA1/L
PB 82 DATA2/L
PB 73 DATA3/L
PB 61 DATA4/L
PB 57 DATA5/L
PB 95 DATA6/L
PB 55 DATA7/L
PB 80 DATA8/L
PB 63 DATA9/L
PB 75 DATA10/L
PB 56 DATA11/L
PB 59 DATA12/L
PB 84 DATA13/L
PB 56 DATA14/L
PB 58 DATA15/L
RECDISIO/H

8835
1D
1E
1F
1G

IB0 IB1 IB2 IB3 IB4 IB5 IB6 IB7 IB8 IB9 IB10 IB11 IB12 IB13 IB14 IB15

LSB

S23E017
C

SEQ. CTRL MODE. PIO COMMANDS. PIO XCVR

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TOLERANCES DECIMAL .XX ±=.01 .XXX ±=.005 .XXXX ±=.0050 FRACTIONAL±=1/64 ANGULAR±=.300

MATERIAL

FINISH

L23X004 1
A23E015

PART NUMBER NEXT ASSEMBLY QTY

DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
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BEDFORD, MASS. 01730

SIZE SHT 1A

SYM REVISION DESCRIPTION APPD DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE DWG NO. S23E017

UNIT INT. SHT 2 OF 19 SHTS

IB (0:15)

PIORDOUTFIF/P

+5V

PA 93

PA 94 DCHPINFIRST/L

PA 92 DCHPOUTLAST/L

PB 17 DCHM0/L

PB 21 DCHM1/L

PB 37 DCHI/P

PA 90 DCHA/N

1K R103

S86 1T

S02 3M

LS11 1R

GTOVCYC

P/1

LS74A 1B

S02 4J

CLKOUTOUTFIF/N

LS08 1M

FILT

S02 3M

LS00 2M

MSB

IB0 IB1 IB2 IB3

IB4 IB5 IB6 IB7

IB8 IB9 IB10 IB11

IB12 IB13 IB14 IB15

LSB

OUTPUT FIFO

S225 2D

S225 2E

S225 2F

S225 2G

P/2

LS20 8C

OROUTFIF/H

S09 3T

DATAVAIL/H PA 86

IROUTFIF/L

OUTPUT FIFO DRIVER

S240 1C

S240 2C

MSB DATA (0:15)

DATA0/L DATA1/L DATA2/L DATA3/L DATA4/L DATA5/L DATA6/L DATA7/L

DATA8/L DATA9/L DATA10/L DATA11/L DATA12/L DATA13/L DATA14/L DATA15/L

LSB

LS14 8T

PE 48 BPARITYER/L

PARERR/H

IBTOCAR/L

S32 3N

LDCARCLRFIF/N

RDBYT1/L

OEINFIFBYTE1/L

RDBYT2/L

OEINFIFBYTE2/L

INFIFTOIB/L

CLKOUTINFIF/N

GPUCLK1

IBTOOUTFIF/L

S02 3M

LS32 2J

CLKINOUTFIF/P

IBTOIMEM/H

PIOWRT/N

LS04 1J

CIOR/L

CLRCAR/P

S23E017

C

OUT FIFO, DATA CHANNEL VGU LOGIC

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TOLERANCES
DECIMAL
.XX +/-.01
.XXX +/-.005
.XXXX +/-.0050
FRACTIONAL +/-1/64
ANGULAR +/-.100

MATERIAL

FINISH

L23X004 1
A23E015 REF

PART NUMBER NEXT ASSEMBLY QTY

DRN S HOSES
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1A

SYM REVISION DESCRIPTION APPD DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE

DWG NO. S23E017

UNIT WT.

SHT 3 OF 19 SHTS

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

IBSRC (0:3)

IBDST (7:10)

ENFIFORD/H

BUSY/H

IBTOCAR/L

IBTOBMAR/L

IBTOBMEM/L

IRINFIF/H

PE 50

BMEMBSY/L

INTERNAL BMEMBSY

P/3

LS74A 1XA

LS32 1W

S00 1X

180 R10

270 R9

LS14 6T

LS14 6T

IBDST7

IBDST8

IBDST9

IBDST10

S04 1Y

B151 2XA

IBSRC0

IBSRC1

IBSRC2

IBSRC3

B151 3XA

CLOCK CONTROL ROM

FIRSTCYC/H

XCYC/H

S10 2V

BUSYWAIT/H

6331-1 2Y

74S74 2Z

DRDISBWRT/H

BMEMORY CONTROL FPLA

82S100 3X

CIOR/L

IROUTFIF/L

FSTMBSY/H

ORINFIF/L

S174 3Y

S174 4W

S174 4XA

28LS31 4ZB

BLDMAR/H PE 8

BLDMAR/L PE 9

BMEMRD/H PE 2

BMEMRD/L PE 3

BMEMWRT/H PE 6

BMEMWRT/L PE 8

CLKO/H

CLKININFIF/P

S88 1T

LS04 6H

DRDISBMC/H

DRDISBRD/H

S23E017 C

DIVIDE BY 2

74S74 2Z

GPUCLK1

GPUCLK2

GPUCLK3

WRITE/N

9MHZ/H

9MHZ/L

18MHZ

18MHZ 1Z OUT

18MHZ/L

BMEM CONTROL CLOCK CONTROL

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MATERIAL		
FINISH	L23X004	1
	A23E015	REF
PART NUMBER	NEXT ASSEMBLY	QTY

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES DECIMAL
XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.30°

DRN B HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE

DWG NO. S23E017

UNIT WT.

SHT 4 OF 19 SHTS

BM (0:15)

③ CLRCAR/P
④ CLKININFIF/P
③ LDCARCLRFIF/N

INPUT FIFO

MSB BM0 BM1 BM2 BM3 — 9D (8225) — P/4 19 — 18

③ OEINFIFBYTE1/L

BM4 BM5 BM6 BM7 — 9E (8225) — P/4 19 — 18

③ CLKOUTINFIF/N

BM8 BM9 BM10 BM11 — 9F (8225) — P/4 19 — 18

③ OEINFIFBYTE2/L

BM12 BM13 BM14 BM15 LSB — 9G (8225) — P/4 19 — 18

LS20 8C: 12, 9, 10, 13 → 8 → ORINFIF/L ④

IRINFIF/H ④

IB (0:23)

BMEMORY ADDRESS COUNTER (CAR)

MSB IB0 IB1 IB2 IB3 — LSB IB23 IB22 IB21 IB20 — 10H (LS193) — P/13 — LSB

IB4 IB5 IB6 IB7 — IB19 IB18 IB17 IB16 — 10Q (LS193) — P/13

IB8 IB9 IB10 IB11 — IB15 IB14 IB13 IB12 — 10F (LB193) — P/13

IB12 IB13 IB14 IB15 LSB — IB11 IB10 IB9 IB8 — 10E (LS193) — P/13 — BADRB

MSB IB7 IB6 IB5 IB4 — 10D (LS193) — BADR5 BADR4 BADR3 BADR2 — MSB

IB2 IB1 IB0 MSB — 12D (LS193) — BADR1 BADR0 — LSB

④ DRDISBRD/H

BADR (0:6) ⑥

BMEMORY READ XCVR

LSB BM15 BM14 BM13 BM12 — 8838 (11H) — LSB BMEMBUS15/L BMEMBUS14/L BMEMBUS13/L BMEMBUS12/L

BM11 BM10 BM9 BM8 — 8638 (11G) — BMEMBUS11/L BMEMBUS10/L BMEMBUS9/L BMEMBUS8/L

BM7 BM6 BM5 BM4 — 8836 (11F) — BMEMBUS7/L BMEMBUS6/L BMEMBUS5/L BMEMBUS4/L

BM3 BM2 BM1 BM0 MSB — 8836 (11E) — MSB BMEMBUS3/L BMEMBUS2/L BMEMBUS1/L BMEMBUS0/L

+5V, 330, R102, R101, 10, 390

LSB BMEMBUS15/L PE 11 — BMEMBUS14/L PE 13 — BMEMBUS13/L PE 15 — BMEMBUS12/L PE 17

BMEMBUS11/L PE 19 — BMEMBUS10/L PE 21 — BMEMBUS9/L PE 23 — BMEMBUS8/L PE 25

BMEMBUS7/L PE 27 — BMEMBUS6/L PE 29 — BMEMBUS5/L PE 31 — BMEMBUS4/L PE 33

S23E017 C

BMEMBUS3/L PE 35 — BMEMBUS2/L PE 37 — BMEMBUS1/L PE 39 — BMEMBUS0/L PE 41

MSB BMEMBUS (0:15)/L ⑥

IN FIFO, CAR, BMEM READ XCVR

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TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0030 FRACTIONAL ±1/64 ANGULAR ±1° .25°

MATERIAL

FINISH

L23X004 1
A23E015 REF

PART NUMBER NEXT ASSEMBLY QTY

DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

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200 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE DWG NO. S23E017

UNIT WT. SHT 5 OF 19 SHTS

IB (0:23)

IBSRC (0:3)

IBSRC (0:3)

IB (0:15)

BMEMORY WRITE DRIVER

MSB

MSB

8838 12E

8838 12F

8838 12G

8838 12H

BMEMBUSD/L
BMEMBUS1/L
BMEMBUS2/L
BMEMBUS3/L
BMEMBUS4/L
BMEMBUS5/L
BMEMBUS6/L
BMEMBUS7/L
BMEMBUS8/L
BMEMBUS9/L
BMEMBUS10/L
BMEMBUS11/L
BMEMBUS12/L
BMEMBUS13/L
BMEMBUS14/L
BMEMBUS15/L

LSB

LSB

DRDISBWRT/H (4)

BMEMBUS (0:15)/L (5)

S240 12C

S240 11D

S240 12C

S240 11D

BMADD/L
BMAD1/L
BMAD2/L
BMCD/L
BMC1/L
BMC2/L
BMC3/L

BADR (0:6) (5)

DRDISBMC/H (4)

BMADD/L PE 44
BMAD1/L PE 4D
BMAD2/L PE 3B
BMCO/L PE 46
BMC1/L PE 47
BMC2/L PE 45
BMC3/L PE 43

L8374 4L

L8374 5L

PIO MAR

IBD
IB1
IB2
IB3
IB4
IB5
IB6
IB7
IB8
IB9
IB10
IB11
IB12
IB13
IB14
IB15

IBSRCD
IBSRC1
IBSRC2
IBSRC3
IBTDIMEM/H (3)(7)(8)(17)
BYTSEL (9)
IADR0
IADR1
IADR2
IADR3
IADR4
IADR5
IADR6
IADR7
IADR8
IADR9

IADR (0:9) (7)(8)(9)

BUSY/H (1)
LDPIDMAR/N (2)
BUSY/L (1)
PIDRD/N (2)

S08 3P

FIRSTCYC/H (4)

74154 2R

SHF1TDIB/L (13)
SHF2TOIB/L (13)
SHF3TOIB/L (14)
SHF4TOIB/L (14)
INF1FTDIB/L (3)
IMEMTDIB/L (7)
ROMTOIB/L (7)(9)
ALUTOIB/L (10)(11)
RATOIB/L (18)
IMARTOIB/L (7)

IBSRC0
IBSRC1
IBSRC2
IBSRC3

IBUS SOURCE DECODE

1-2824 7S

AD (10)(11)
A1 (10)(11)
A2 (10)(11)
A3 (10)(11)

P/5

S175 7U

LS00 7V

LS00 7V

ENFIFORD/H (4)
ANYENTRY/H (15)

CIOR/L (1)

IBDST (7:10) (16)

GPUCLK2 (4)

S138 7X

S138 7W

IBDST6
IBDST9
IBDST10

P/6

IBDST7

IBTOBMAR/L (4)
IBTDBMEM/L (4)
IBTOCAR/L (3)(4)
IBTOOUTFIF/L (3)
INSTEND/L (2)
TASKTERM/L (2)
DIVIDE/L (10)
MULGD/L (12)

DESTINATION DECODE

IMTDMUL1/L (13)
IMTOMUL2/L (13)
IMTOMUL3/L (14)
IMTDMUL4/L (14)

S23E017
C

PIOMAR, IBUS SOURCE, DESTINATION DECODE, AND BMEM WRITE DRIVER

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TOLERANCES DECIMAL .XX ±0.01 .XXX ±0.005 .XXXX ±0.0050 FRACTIONAL ±1/64 ANGULAR ±0.30

MATERIAL

FINISH

L23X004 1

A23E015

PART NUMBER NEXT ASSEMBLY QTY

DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SIZE INT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE

DWG NO. S23E017

UNIT INT.

SHT 6 OF 19 SHTS

COMPUTERVISION CORP.
300 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

IADR (0:9)
MADR (0:9)
IADR (0:9)
IADR (6:9)
IMAR
IMAR (0:9)
IADR MUX
IMEM BYTE 1
RDBYT2/L
LS32
4N
IB12
IB13
IB14
IB15
1/0D
1/0C
1/0B
1/0A
8566
4M
IMARO
IMAR1
IMARTOIB/L
RDBYT3/L
IB16
IB17
IB15
IB19
8555
5M
IMAR2
IMAR3
IMAR4
IMAR5
IB20
IB21
IB22
IB23
8556
5N
IMAR7
IMAR6
IMAR9
IBTOIMAR/L
IB (12:24)
GPUCLK2
INCIMAR/L
SADRO
SADR1
SADR2
SADR3
BUSY/L
MADRO
IMARO
MADR1
IMAR1
MADR2
IMAR2
MADR3
IMAR3
MADR4
IMAR4
MADR5
IMAR5
6257
7M
6M
6N
IADRO
IADR1
IADR2
IADR3
IADR4
IADR5
SEL5
S04
7P
MADR6
IMAR6
MADR7
IMAR7
MADR9
IMAR9
74S251
7N
IADR6
IADR7
IADR9
IADR2
IADR3
IADR4
IADR5
IADR6
IADR7
IADR8
IADR9
IB0
IB1
IB2
IB3
IB4
IB5
IB6
IB7
93422
6J
7J
6K
7K
6L
7L
OE
W
CS1
CS2
IM0
IM1
IM2
IM3
IM4
IM5
IM6
IM7
IBTOIMEM/H
WRTBYT1/H
WRITE/N
PIOWRT/N
RDBYT1/L
S10
3K
B10
6J
S02
4J
6H
IMEMWRT/H
S241
7H
IB (0:7)
IM (0:7)
IADR1
IADR1/L
IMEMTOIB/L
ROMTOIB/L
S05
3P
MORRTOIB/L
ROMTOIB/H
S23E017
C
INTERNAL ADDRESS GENERATION
AND IMEM BYTE 1

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MATERIAL
FINISH
PART NUMBER
L23X004
A23E015
NEXT ASSEMBLY
QTY 1
TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.30
DRN
CHK
ENGR
PROJ
MFG
SIGNATURE
DATE
REMOVE ALL BURRS AND SHARP EDGES
SEE SHT 1A
SYM REVISION DESCRIPTION APPD DATE
TITLE GPU SCHEMATIC DIAGRAM
SCALE
DWG NO. S23E017
UNIT WT.
SHT 7 OF 19 SHTS

COMPUTERVISION CORP.
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BEDFORD, MASS. 01730

IADR (0:9)

IMEM BYTE 2

IMEM BYTE 3

93422 8J

93422 8L

93422 9J

93422 9L

93422 8K

93422 9K

93422 10J

93422 10L

93422 10K

93422 11J

93422 11L

93422 11K

S241 9H

S241 8H

S10 6J

S02 4J

S04 6H

IADR0

IADR1/L

WRTBYT2/H

IMEMWRT/H

IBTOIMEM/H

RDBYT2/L

MORRTOIB/L

ROMTOIB/H

WRTBYT3/H

RDBYT3/L

IM (8:23)

IB (8:23)

S23E017

C

IMEM BYTE 2 AND 3

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MATERIAL

FINISH

PART NUMBER L23X004 1

NEXT ASSEMBLY A23E015

QTY

COMPUTERVISION CORP.
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BEDFORD, MASS. 01730

TOLERANCES
DECIMAL
XX +-.01
XXX +-.005
XXXX +-.0010
FRACTIONAL=+-1/64
ANGULAR=+-.100

DRN S HOSSE

REF

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SIZE SHT 1A

SYM REVISION DESCRIPTION APPD DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE

DWG NO. S23E017

UNIT WT.

SHT 8 OF 19 SHTS

READ TRANSFER CONTROL ROM

WRITE CONTROL ROM

RDBYT1/L
RDBYT2/L
RDBYT3/L

RDSEL0
RDSEL1
BUSY/H
BYTSEL
PIORD/N

WRTSEL0
WRTSEL1
WRTSEL2

WRTBYT1/L
WRTBYT1/H
WRTBYT2/L
WRTBYT2/H
WRTBYT3/L
WRTBYT3/H
WRTBYT12/L

ROMTOIB/L

IADR (1:9)

IB (0:23)

1-2XFER

1-3XFER

2-3XFER

CONSTANTS ROM BYTE 1

CONSTANTS ROM BYTE 2

CONSTANTS ROM BYTE 3

IM (0:23)

S23E017 C

IBUS TRANSFER CONTROL AND CONSTANTS ROM

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MATERIAL			
FINISH	L23X004	1	
	A23E015	REF	
PART NUMBER	NEXT ASSEMBLY	QTY	

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES DECIMAL
.XX +-.01
.XXX +-.005
.XXXX +-.0038
FRACTIONAL +-1/64
ANGULAR +-.300

DRN B HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE DWG NO. S23E017

UNIT WT. SHT 9 OF 19 SHTS

A (0:3)

ALU (0,1,2,4,5,7)

IB (0:7)

B (0:3)

ALU (0:8)

IB (0:7)

ALU INSTRUCTION MUX

ALUPL6

BUSY/H

ALUPL6

ALUPL3

CINPL

DIVIDE/L

QRAM8-0

TB7

BPL (0:3)

IADR (6:9)

B-REGISTER SELECT MUX

GO

PO

ALUTOIB/L

RDBYT1/L

GPUCLK2

WRTBYT1/L

FBYT2=0/H

FBYT3=0/H

BSEL

SLICE 0 (OVERFLOW)

SLICE 1

SLICE 2

2901-A

5Z

5Y

5X

7ZA

7Y

7Z

2902-A

S00

S04

S32

S09

125

1K R6

470 R11

P/S

Q6

F3

CIN

Q3-2

RAM3-2

F=0/H

OVR1/H

S23E017 C

OVERFLOW SLICE AND ALU BYTE 1

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MATERIAL

FINISH

PART NUMBER L23X004 1

NEXT ASSEMBLY A23E015 QTY

TOLERANCES DECIMAL XX ±.01 XXX ±.005 XXXX ±.0030 FRACTIONAL ±1/64 ANGULAR ±.30

DRN S HOSSE

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1A

SYM REVISION DESCRIPTION APPD DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE DWG NO. S23E017

UNIT WT. SHT 10 OF 19 SHTS

COMPUTERVISION CORP.
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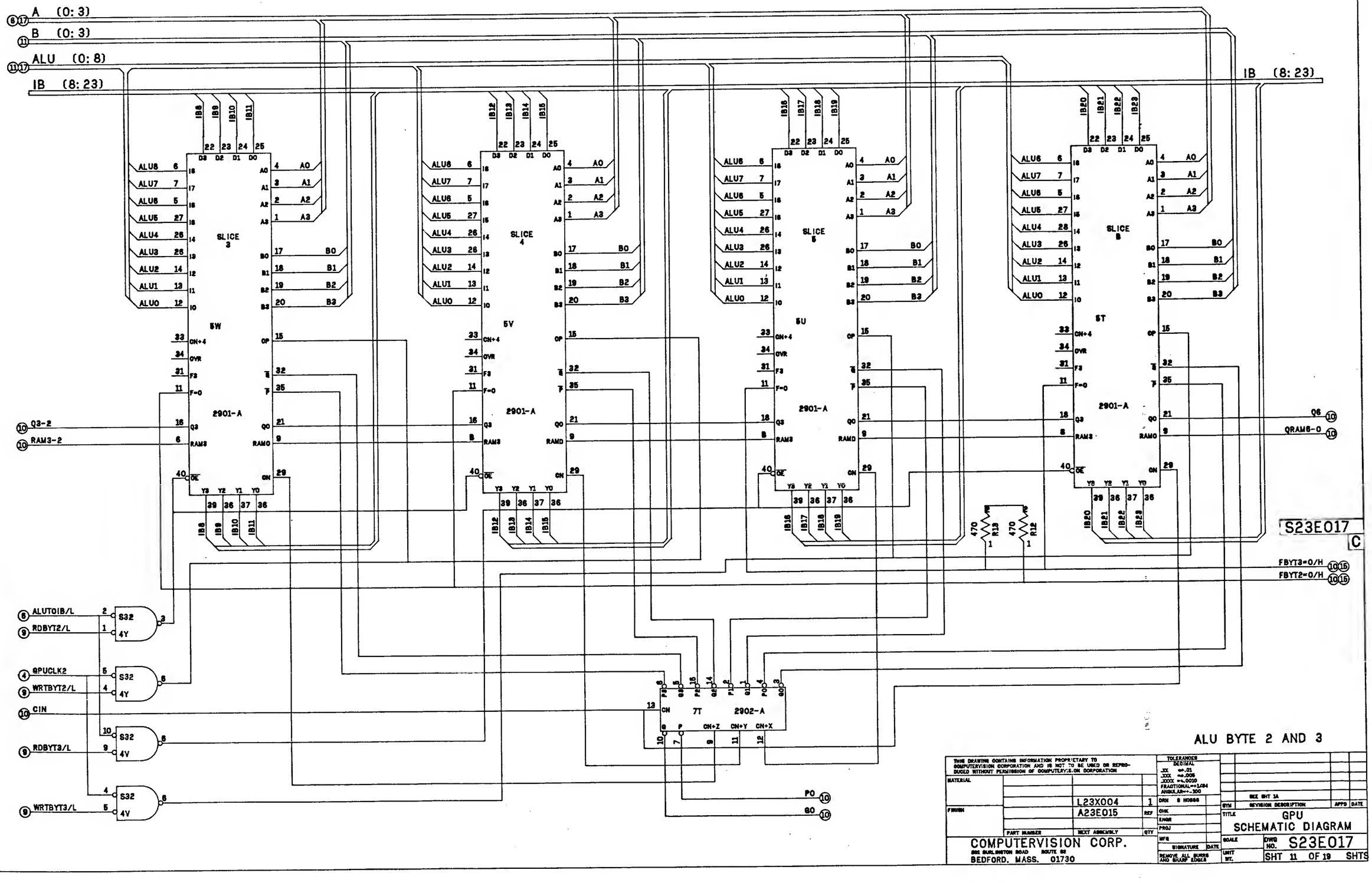
BEDFORD, MASS. 01730


A (0:3)
B (0:3)
ALU (0:8)
IB (8:23)
IB (8:23)
SLICE 3
SLICE 4
SLICE 5
SLICE 6
5W
5V
5U
5T
2901-A
7T 2902-A
Q3-2
RAM3-2
Q6
QRAM6-0
FBYT3-O/H
FBYT2-O/H
ALUTOIB/L
RDBYT2/L
GPUCLK2
WRTBYT2/L
CIN
RDBYT3/L
WRTBYT3/L
S32
470 R13
470 R12
PO
GO
S23E017
C
ALU BYTE 2 AND 3
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
L23X004
A23E015
GPU
SCHEMATIC DIAGRAM
DWG NO. S23E017
SHT 11 OF 19 SHTS

IB (18:23)

MULTIPLIER INSTRUCTION REGISTER

SIGN EXTEND

MULTIPLIER BUSY

MULTIPLIER COUNT

SHIFTER MUX

MULTIPLIER CONTROL

S23E017 C

CLKO/H
9MHZ/L
18MHZ
9MHZ/H
MULGO/L
18MHZ/L
CIOR/L

IB19
IB18
IB23
IB22
IB21
IB20

CLKSIGNX
CLKMUL
MULBSY/L
CLRMUL1/L
CLRMUL2/L

BA0
BA1
BA2
P/2

SOBYT12
S1BYT12
SOBYT3
S1BYT3
FSTMBSY/H

WRTBYT12/L
WRTBYT3/L
IBSRC0
IBSRC1

MBIT1
SBIT1
MBIT2
SBIT2
MBIT3
SBIT3
MBIT4
SBIT4

SHFIN1
SHFIN2
SHFIN3
SHFIN4

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MATERIAL	L23X004	1	DRN S HOBBS
FINISH	A23E015	REF	CHK
			ENGR
			PROJ
PART NUMBER	NEXT ASSEMBLY	QTY	MFG

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES DECIMAL: .XX ±.01, .XXX ±.005, .XXXX ±.0020, FRACTIONAL ±1/64, ANGULAR ±.30

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE

DWG NO. S23E017

UNIT WT.

SHT 12 OF 19 SHTS

SHIFTER 1

MULTIPLIER 1

IB (0:23)

IM (0:23)

SHFIN1

SHFITOIB/L

IMTOMUL1/L

IBTOSHF1/L

CLRMUL1/L

MBIT1

SBIT1

SHIFTER 2

MULTIPLIER 2

SHFIN2

SHF2TOIB/L

IMTOMUL2/L

IBTOSHF2/L

MULBSY/L

18MHZ

QPUCLK1

ROBYT1/L

RDBYT2/L

S1BYT12

S0BYT12

RDBYT3/L

S1BYT3

S0BYT3

CLKSIGNX

CLRMUL2/L

CLKMUL

MBIT2

SBIT2

S23E017

C

MULTIPLIER/SHIFTER
1 AND 2

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MATERIAL			
FINISH		L23X004	1
		A23E015	
	PART NUMBER	NEXT ASSEMBLY	QTY

TOLERANCES
DECIMAL
.XX +-.01
.XXX +-.005
.XXXX +-.0050
FRACTIONAL +-1/64
ANGULAR +-.100

DRN G HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU
SCHEMATIC DIAGRAM

SCALE

DWG NO. S23E017

UNIT WT.

SHT 13 OF 19 SHTS

SHIFTER 3

MULTIPLIER 3

IB (0:23)

IM (0:23)

SHFIN3

SHF3TOIB/L

IMTOMUL3/L

IBTOSHF3/L

MBIT3

SBIT3

SHIFTER 4

MULTIPLIER 4

SHFIN4

SHF4TOIB/L

IMTOMUL4/L

IBTOSHF4/L

MULBSY/L

18MHZ

GPUCLK1

RDBYT1/L

RDBYT2/L

S1BYT12

SOBYT12

RDBYT3/L

S1BYT3

SOBYT3

CLKSIGNX

CLRMUL2/L

CLKMUL

MBIT4

SBIT4

S23E017

C

MULTIPLIER/SHIFTER
3 AND 4

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MATERIAL		
FINISH	L23X004	1
	A23E015	REF
PART NUMBER	NEXT ASSEMBLY	QTY

TOLERANCES
DECIMAL
.XX +-.01
.XXX +-.005
.XXXX +-.0030
FRACTIONAL +-1/64
ANGULAR +-.100

DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU
SCHEMATIC DIAGRAM

SCALE

DWG NO. S23E017

UNIT WT.

SHT 14 OF 19 SHTS

IB (0:16)

TADR (0:3)

TB (0:7)

TEST BYTE 1

TEST BYTE 2

TEST BYTE SELECTOR

FLAGS

LATCHED CONDITIONS

DYNAMIC CONDITIONS

TEST BYTE GENERATION

S23E017 C

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MATERIAL		
FINISH	L23X004 1	
	A23E015 REF	
PART NUMBER	NEXT ASSEMBLY	QTY

COMPUTERVISION CORP.
901 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0030
FRACTIONAL ±1/64
ANGULAR ±.30

DRN S MOSES
CHK
ENGR
PROJ
MFR
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHT 1A		

TITLE GPU SCHEMATIC DIAGRAM

SCALE DWG NO. S23E017

UNIT WT. SHT 15 OF 19 SHTS

BA (0:3)

RB84 RB85 RB86 RB87 GPUCLK1

26S16 6S

SA8 SA9 SA10 SA11

MULTIWAY BRANCH ROM

6301-1 3S

TB4 TB5 TB6 TB7

TB0 TB1 TB2 TB3 TB4 TB5 TB6 TB7

DECODE FPLA

82S100 4R

BA4 BA5 BA6 BA7 BA8 BA9 BA10 BA11

B14 TSTBIT2 TSTBIT1 TSTBIT0

TB (0:7)

TEST BIT MUX

S151 2S

S86 1T

R871 R872 R873 R874 CLRUADR/L INVCC/H

S175 8R

2910 SR

U-PROGRAM SEQUENCER

S04 4T

FULL PL MAP VECTOR NLO

P/10

BAPL7 BAPL6 BAPL5 BAPL4 RAT01B/L

LS244 5B LS244 4S

RA (0:11)

IB (3:15)

PAGE 5P

S23E017 C

U-PROGRAM SEQUENCE CONTROL

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MATERIAL	
FINISH	
PART NUMBER	L23X004
NEXT ASSEMBLY	A23E015
QTY	1

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±.100

DRN S HOBBS

DMK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU SCHEMATIC DIAGRAM

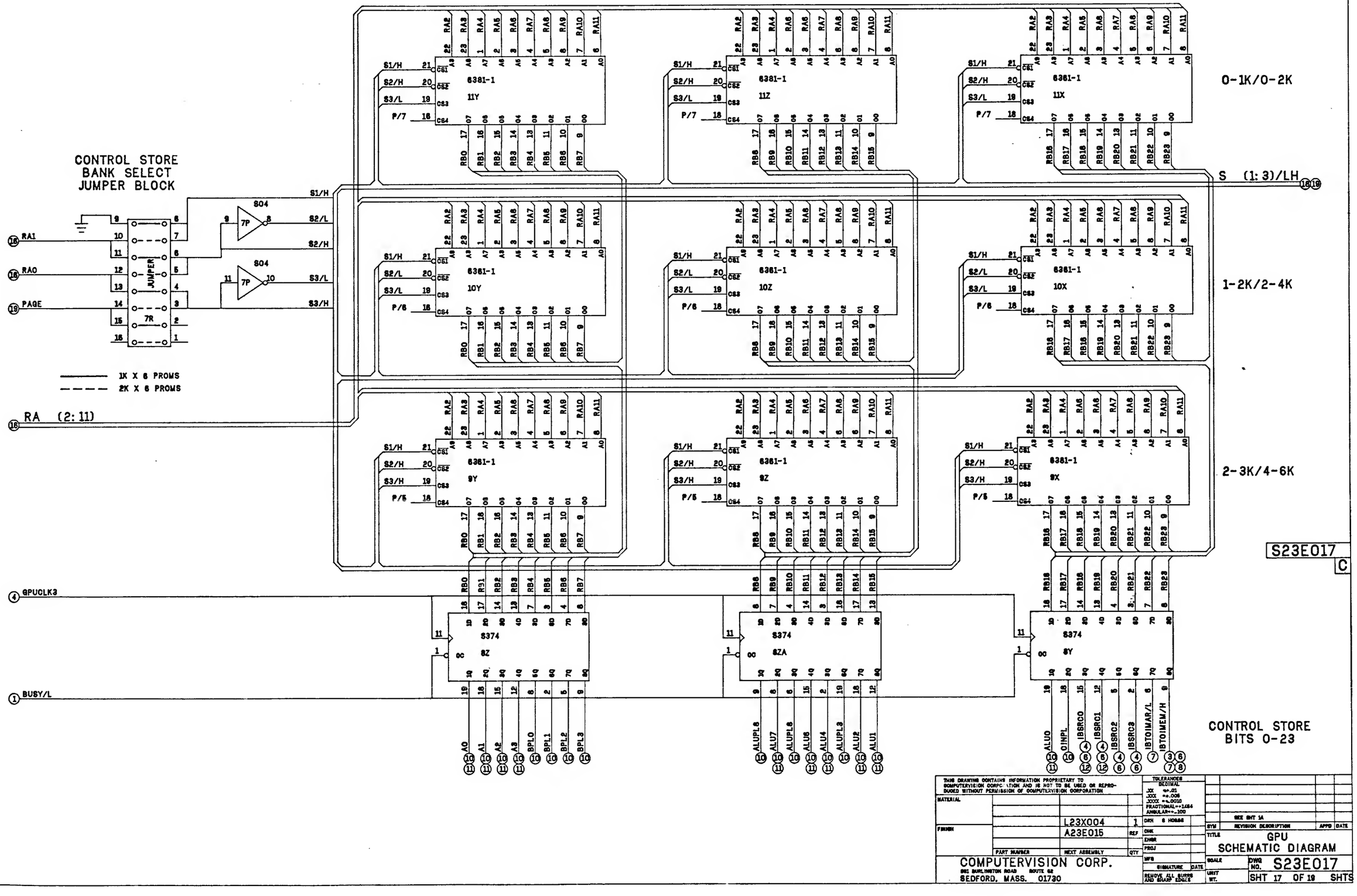
SCALE

DWG NO. S23E017

UNIT WT.

SHT 18 OF 19 SHTS

COMPUTERVISION CORP.
300 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730



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TOLERANCES
DECIMAL
XX ±0.01
.XXX ±0.005
.XXXX ±0.0010
FRACTIONAL ±1/64
ANGULAR ±1.100

MATERIAL				
FINISH		L23X004	1	DRN S HOBBS
		A23E015	REF	CHK
				ENGR
				PROJ
PART NUMBER	NEXT ASSEMBLY		QTY	MFG

SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
961 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE
GPU
SCHEMATIC DIAGRAM

SCALE
DWG NO. S23E017

UNIT
WT.
SHT 17 OF 19 SHTS

0-1K/0-2K

1-2K/2-4K

2-3K/4-6K

RA (2:11)
(18)

S (1:3)/LH
(17)

(4) GPUCLK3

8381-1 11W
8381-1 11V
8381-1 11N
8381-1 11P
8381-1 10W
8381-1 10V
8381-1 10N
8381-1 10P
8381-1 9W
8381-1 9V
8381-1 9N
8381-1 9P

S374 8X
S374 8W
S374 8N
S374 8P

IBDBT7
IBDSTB
IBDSTB
IBDSTB
IBOBTIO
RDBELO
RDBEL1
WRTSELO
WRTSEL1
WRTSEL2
BADRO
BADR1
BADR2
BADR3
MADRO
MADR1
MADR2
MADR3
MADR4
MADR5
MADR6
MADR7
MADR8
MADR9
INVOO/H
XOYO/H
BSEL
SELB

S23E017
C

CONTROL STORE
BITS 24-55

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MATERIAL
FINISH
PART NUMBER L23X004 | NEXT ASSEMBLY A23E015 | QTY 1

TOLERANCES DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.100

DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU SCHEMATIC DIAGRAM

SCALE
DWG NO. S23E017
UNIT WT.
SHT 18 OF 19 SHTS

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

0-1K/0-2K

1-2K/2-4K

2-3K/4-6K

RA (2:11)
16

S (1:3)/LH
17

GPUCLK3
4

RB(71:74,84:87)
16

CONTROL STORE
BITS 56-87

S23E017
C

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MATERIAL			
FINISH	L23X004	1	DRN B HOBBS
	A23E015	REF	CHK
			ENGR
			PROJ
PART NUMBER	NEXT ASSEMBLY	QTY	MFG

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±.100

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1A

SYM	REVISION DESCRIPTION	APPD	DATE

COMPUTERVISION CORP.
900 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TITLE GPU SCHEMATIC DIAGRAM

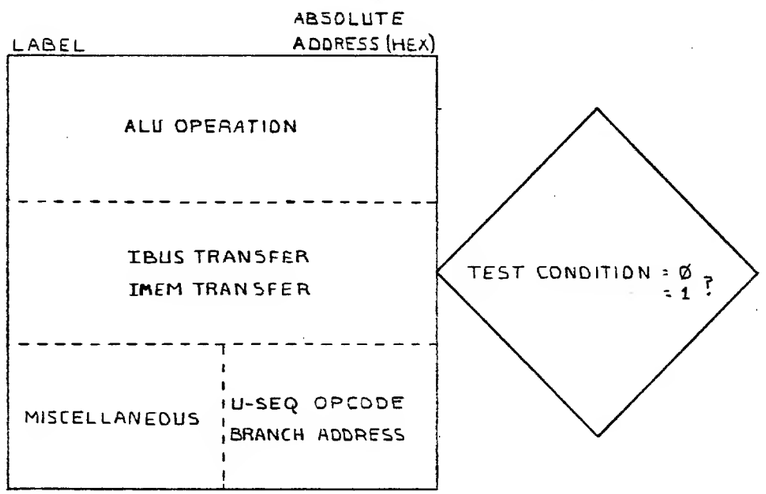
SCALE

DWG NO. S23E017

LIMIT WT.

SHT 19 OF 19 SHTS

GPU Microprogram Flow Charts



ALU OPERATION

R (OP) S , SHIFT → DEST
- R = (RA, Ø, IB)
  - RA = REG FILE A-ADDR
  - IB = IBUS DATA
- S = (RA, RB, Ø, Q)
  - RB = REG FILE B-ADDR
  - Q = Q REG
- (OP) = (+, -, OR., AND., EXOR., EXNOR)
- SHIFT = (RS, LS) IF A SHIFT EXISTS
  - RS = RIGHT SHIFT
  - LS = LEFT SHIFT
- DEST = (RB, Q, F)
  - F = ALU OUTPUT

NOTE: WHEN RB OR Q IS SELECTED AS THE ALU DEST, THE RESULT WILL ALSO APPEAR AT THE F OUTPUT

IBUS TRANSFER (IB)

IBUS SOURCE: RDSEL → IBUS DEST: WRTSEL

IBUS SOURCES = SHF1, SHF2, SHF3, SHF4, INFIFO, ALU, RA, IMAR, IMEM - [SADR: MADR] IMEM, ROM - [SADR: MADR] ROM

RDSEL = (RDALL, RD1, RD2, RD3)

IBUS DESTINATIONS = BMAR, BMEM, CAR, OUTFIFO, IMAR, IMEM - [SADR: MADR] IMEM, TEST - [TADR] TEST, SHF1, SHF2, SHF3, SHF4

WRTSEL = (WRTØ, WRT1, WRT2, WRT3, WRT12, WRT13, WRT23, WRTALL)

IMEM TRANSFER

[SADR: MADR] IMEM → IMEM DESTINATION

IMEM DESTINATIONS = MUL1, MUL2, MUL3, MUL4

U-SEQ OPCODE

SEE THE U-CODE LISTING FOR THE 16 POSSIBLE OPCODES AND THEIR DEFINITIONS

BRANCH ADDRESS

:XYZ - REPRESENTS THE LABEL THAT A JUMP WILL GO TO UPON EXECUTION

( ) - REPRESENTS AN ABSOLUTE NUMBER

MISCELLANEOUS

TASKTERM
LDCOND
XCYC
INCIMAR
INV
MULGO (OP)
(OP) = (LSHF, RSSEX, MULT)
DIVIDE
CLRFLAGS
FLAG (X) = (Ø, 1)
X = Ø, 1, 2, ..., 7
INSTEND
IADRB
P2

TEST CONDITION

TEST BYTE 1
[TADR] TSTBYT1 (TSTBIT) = (Ø, 1) ?

TEST BYTE 2
[TADR] TSTBYT2 (TSTBIT) = (Ø, 1) ?

FLAGS TEST BYTE
FLAG (X) = (Ø, 1) ?
X = Ø, 1, 2, ..., 7

LATCHED CONDITIONS TEST BYTE
F = Ø ?
FBYT2 = Ø ?
FBYT3 = Ø ?
F3 = 1 ?
OVR1 = 1 ?

DYNAMIC CONDITIONS TEST BYTE
F = Ø ?
F3 = 1 ?
IBØ = 1 ?
IMØ = 1 ?

NOTE: THESE ARE DENOTED BY THE WORD "DYNAMIC" WITHIN THE TEST DIAMOND

DS 21E1065
B

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CHK		10-79
ENGR		10-79
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MFG		

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SYM	REVISION DESCRIPTION	CHK	APPD	DATE
B	ECO #3421			
A	REL. ECO 3283			

TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: —

DWG NO. DS21E1065

UNIT WT. —

SHEET 1 OF 30 SHEETS

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U-SEQ TEST

START UP Ø

[MADR:HDA] IMEM: RD2
→[Ø] TEST:WRT1

TASK COMMAND REG BYTE 2 TO TEST WORD Ø BYTE 1

1

[MADR:HDA] IMEM:RD1
→[Ø] TEST:WRT 2

TASK COMMAND REG BYTE 2 TO TEST WORD Ø BYTE 1

2

CJP :DIAG

IF DIAGNOSTIC BIT SET, JUMP TO: DIAG OTHERWISE CONTINUE

[Ø] TSTBYT2 (7) =1 ?

TRUE

FALSE

(JJ) SH. 30

DIAG 1Ø

JUMP :SEQ A

JUMP TO SEQ A

SEQ A 12

PASS CJS :SEQ B

JUMP TO SEQ B, PUSH ADDR HI3 ONTO STACK

SEQ B 14

PASS CJPP :SEQ C

JUMP TO SEQ C, POP ADDR HI3 FROM STACK

SEQ C 16

PASS CJS :SEQ D

JUMP TO SEQ D, PUSH ADDR HI7 ONTO STACK

3

[MADR:HDA] IMEM: RD3
→[Ø] TEST:WRT2

TASK COMMAND REG BYTE 3 TO TEST WORD Ø BYTE 2

4

[MADR:HD2] IMEM
→CAR

LDCOND JUMP :NEXT

PROGRAM COUNTER (PC) TO CAR

START EXECUTION OF GPU INSTRUCTIONS

ERR I 11

TASKTERM JUMP :ERRI

IF U-SEQ DID NOT JUMP, TASKTERM

ERRIA 13

TASKTERM JUMP :ERRIA

IF U-SEQ DID NOT JUMP, TASKTERM

ERRIB 15

TASKTERM JUMP :ERRIB

IF U-SEQ DID NOT JUMP, TASKTERM

SEQ D 18

PASS CJS :SEQE

JUMP TO SEQC, PUSH ADDR HI9 ONTO STACK

SEQE 1A

PASS CJPP :SEQE+2

JUMP TO SEQE+2 POP ADDR HI9

1C

PASSCRTN

POP AND JUMP TO ADDR HI7

17

JUMP :SEQF

JUMP TO SEQ F

SEQ F 1E

JMAP (HF)

ENABLE FPLA, BA8:11= HF, T8Ø:7 = DON'T CARE FPLA OUTPUT=HC

DEC DIAG FPLA DECISION

C

JUMP :SEQF+2

JUMP TO SEQF+2

(A) SH.3

ERRIC 19

TASKTERM JUMP :ERRIC

IF U-SEQ DID NOT JUMP OR POP CORRECTLY, TASKTERM

ERRID 1B

TASKTERM JUMP :ERRID

IF U-SEQ DID NOT JUMP, TASKTERM

ERRIE 1D

TASKTERM JUMP :ERRIE

IF U-SEQ DID NOT JUMP, TASKTERM

ERRIF 1F

TASKTERM JUMP :ERRIF

IF U-SEQ DID NOT JUMP, TASKTERM

CHECK FOR DIAGNOSTIC BIT SET
TEST U-SEQ FUNCTIONALITY INCLUDING DECODE FPLA

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B

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FLAGS BYTE TEST
INV BIT TEST

TEST EACH BIT OF THE FLAGS BYTE AND EACH BIT OF THE TEST BUS FOR Ø AND FOR 1. TEST INV BIT.

20
PASS CJV (HF)
ENABLE MULTIWAY BRANCH ROM,
BA8:11 = HF,
TB 4:7 = DONT CARE,
OUTPUT = HB

MULTIWAY BRANCH ROM DECISION

8
JUMP :SEQF+4
JUMP TO SEQF+4

22
FLAG(Ø)=Ø
CLR FLAG Ø

23
CJP :ERR1H
TEST FLAGØ FOR Ø

FLAG(Ø)=1?
FALSE
TRUE

24
FLAG(Ø)=1
SET FLAG Ø

A SH.2

ERR1G 21
TASKTERM JUMP :ERR1G
IF U-SEQ DID NOT JUMP, TASKTERM

B SH. 3,4,5

ERR1H 13D
TASKTERM JUMP :ERR1H
IF ANY FLAG BIT OR TEST BUS BIT IS IN ERROR, OR THE INV BIT IS IN ERROR, THEN TASKTERM

25
INV CJP :ERR1H
TEST FLAG Ø FOR 1

FLAG(Ø)=1?
TRUE
FALSE
B SH.3

26
FLAG(1)=Ø
CLR FLAG 1

27
CJP :ERR1H
TEST FLAG1 FOR Ø

FLAG(1)=1?
FALSE
TRUE
B SH.3

28
FLAG(1)=1
SET FLAG 1

29
INV CJP :ERR1H
TEST FLAG1 FOR 1

FLAG(1)=1?
TRUE
FALSE
B SH.3

C SH.4

DS21E1065
B

CHECK MULTIWAY BRANCH ROM,
START FLAGS BYTE TEST,
TEST INV BIT

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TITLE
GPU MICRO PROGRAM FLOW CHARTS

SCALE X
DWG NO. DS21E1065
UNIT WT. X
SHEET 3 OF 30 SHEETS

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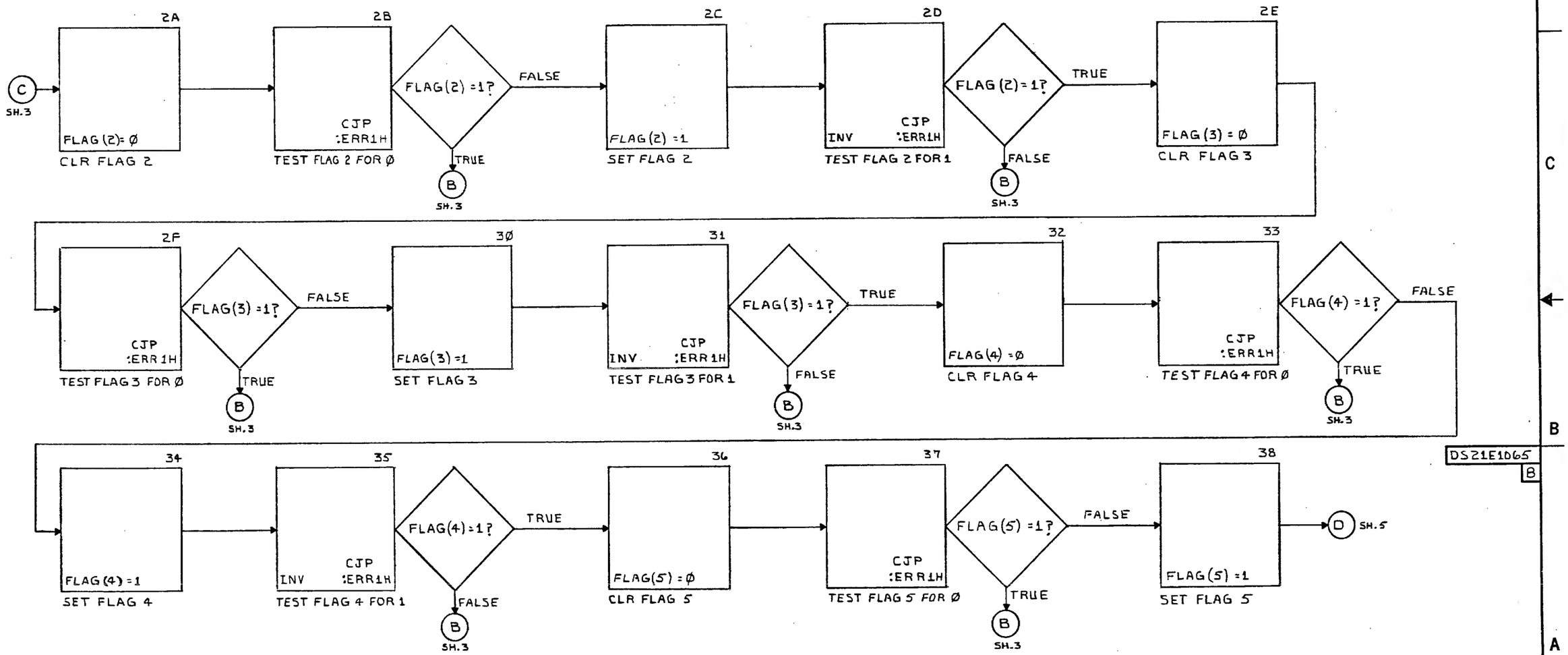

DS21E1065
B

CONTINUE FLAGS BYTE TEST

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SCALE: X
DWG NO. DS21E1065
UNIT WT. X
SHEET 4 OF 30 SHEETS

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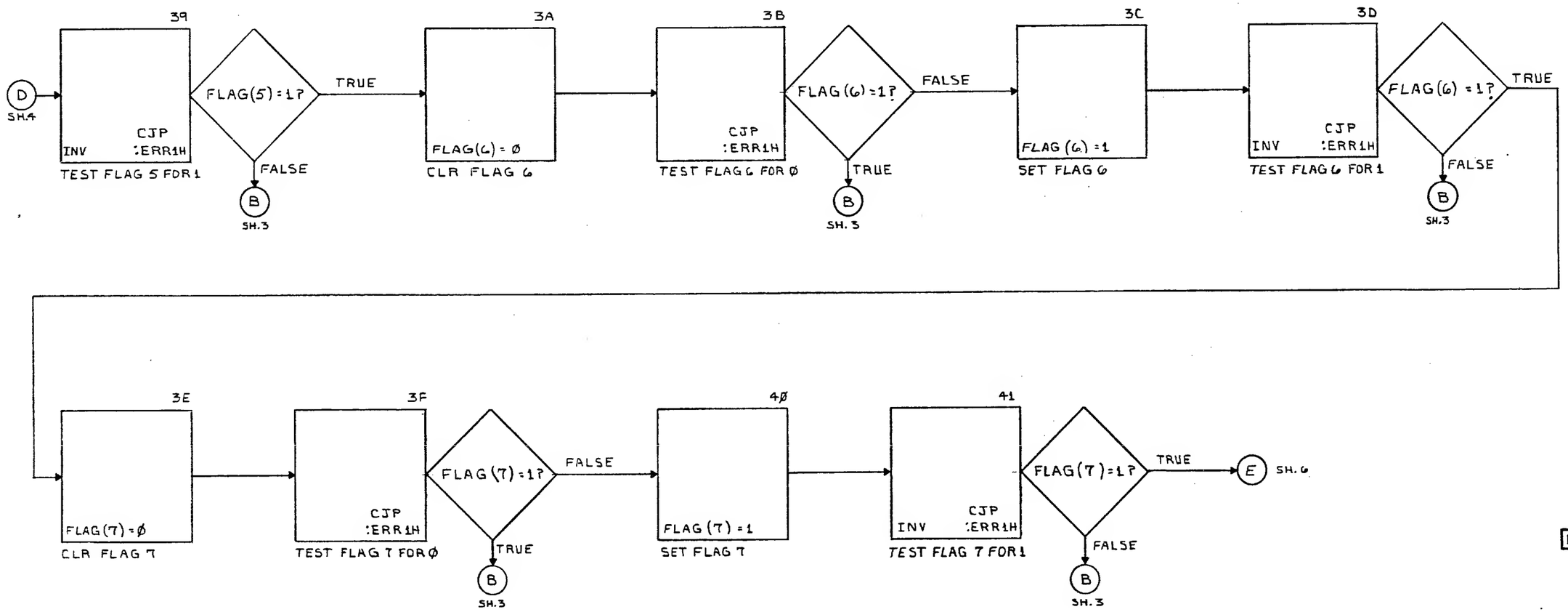

DS21E1065
B

FINISH FLAGS BYTE TEST

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SHEET 5 OF 30 SHEETS

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WRITE CTRL ROM TEST → CHECK TO INSURE THAT ROM DATA CAN BE WRITTEN INTO BYTES 1 AND 2 OF THE TEST BYTE FILE (THIS VERIFIES WRT1 AND WRT2)

42 — [MADR:H2Ø] ROM [HF] TEST — Ø TO TEST WORD F

43 — CJP :ERR2 — TEST BIT Ø OF BYTE 1 WORD F FOR Ø

[HF] TSTBYT1(Ø) =1? — FALSE / TRUE

44 — CJP :ERR3 — TEST BIT 1 OF BYTE 2 WORD F FOR Ø

[HF] TSTBYT2(1) =1? — FALSE / TRUE

45 — [MADR:H21] ROM [HF] TEST — H8Ø4ØØØ TO TEST WORD F

46 — INV CJP :ERR2 — TEST BITØ OF BYTE 1 WORD F FOR 1

[HF] TSTBYT1(Ø) =1? — TRUE / FALSE

ERR2 13E — JUMP TASKTERM:ERR2 — IF WRITING TO BYTE 1 IS IN ERROR, TASKTERM

ERR3 13F — JUMP TASKTERM:ERR3 — IF WRITING TO BYTE 2 IS IN ERROR, TASKTERM

47 — INV CJP :ERR3 — TEST BIT 1 OF BYTE 2 WORD F FOR 1

[HF] TSTBYT2(1) =1? — FALSE / TRUE

48 — [MADR:H2Ø] ROM [HF] TEST:WRTØ — WRTØ ⟶ WRITE NO BYTES, SO THIS IS A NOP

49 — INV CJP :ERR2A — TEST BITØ OF BYTE 1 WORD F FOR 1

[HF] TSTBYT1(Ø) =1? — TRUE / FALSE

4A — INV CJP :ERR3A — TEST BIT 1 OF BYTE 2 WORD F FOR 1

[HF] TSTBYT2(1) =1? — TRUE → (F) SH. 7 / FALSE

ERR2A 140 — JUMP TASKTERM:ERR2A — IF WRTØ DID NOT INHIBIT WRITING TO BYTE 1, TASKTERM

ERR3A 141 — JUMP TASKTERM:ERR3A — IF WRTØ DID NOT INHIBIT WRITING TO BYTE 2, TASKTERM

(E) SH. 5

TEST WRITE CTRL ROM BYTES 1 AND 2, SIMULTANEOUSLY, CHECK TEST BYTE FILES

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TITLE: GPU MICROPROGRAM FLOW CHARTS

DWG NO. DS21E1065

SHEET 6 OF 30 SHEETS

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TEST BYTE FILE ADDRESS TEST → CHECK TEST FILE ADDRESS LINES

F
SH. 6

4B
[MADR:H2Ø] ROM→
[HF] TEST
Ø TO TEST WORD F

4C
[MADR:H21] ROM→
[HE] TEST
H8Ø4Ø TO TEST WORD E

4D
[MADR:H21] ROM→
[HD] TEST
H8Ø4Ø TO TEST WORD D

4E
[MADR:H21] ROM→
[HB] TEST
H8Ø4Ø TO TEST WORD B

4F
[MADR:H21] ROM→
[7] TEST
H8Ø4Ø TO TEST WORD 7

5Ø
CJP :ERR4
TEST BIT Ø OF BYTE 1 WORD F FOR Ø

[HF] TSTBYT1 (Ø) =1?
FALSE
TRUE

READ BYTE 3 TEST → CHECK BYTE3 TO BYTE1, AND BYTE3 TO BYTE2 DATA TRANSFERS

51
CJP :ERR4
TEST BIT 1 OF BYTE 2 WORD F FOR Ø

[HF] TSTBYT2(1) =1?
FALSE
TRUE

52
[MADR:H2A] ROM:RD3 →[HF] TEST
HCØCØCØ TO TEST WORD F (ROM LOC H2A=HØØØØCØ)

53
INV CJP :ERR5
TEST BITØ OF BYTE 1 WORD F FOR 1

[HF] TSTBYT1 (Ø) =1?
TRUE
FALSE

54
INV CJP :ERR5A
TEST BIT 1 OF BYTE 2 WORD F FOR 1

[HF] TSTBYT2(1) =1?
TRUE
FALSE

G
SH.8

ERR4 142
JUMP TASKTERM :ERR4
IF ANY ADDRESS LINE FOR THE TEST BYTE FILE IS IN ERROR, TASKTERM

ERR5 143
JUMP TASKTERM :ERR5
IF BYTE 3-1 TRANSFER IN ERROR, TASKTERM

ERR5A 144
JUMP TASKTERM: ERR5A
IF BYTE 3-2 TRANSFER IN ERROR, TASKTERM

DS21E1065
B

CHECK TEST BYTE FILE ADDRESSING, TEST READ CTRL ROM BYTE 3

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TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE —
DWG NO. DS21E1065
UNIT WT. —
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WRITE CTRL ROM TEST → CHECK TO INSURE THAT ROM DATA CAN BE WRITTEN INTO BYTE 3 OF THE IMEM (THIS VERIFIES WRT 3)

55 — [MADR:H22] IMEM:RD3 → [2] TEST
IMEM ADDR H22 BYTE 3 TO TEST WORD 2 CONTENTS UNKNOWN

56 — CJP :WRTA
TEST BIT2 OF BYTE1 WORD 2 FOR Ø. IF BIT 2=Ø, WRITE A 1 INTO BIT 2. IF BIT2=1, WRITE A Ø INTO BIT 2.

[2] TSTBYT1 (2) =1?
FALSE
TRUE

57 — [MADR:H22] ROM → IMEM
HØØØØ2Ø TO IMEM ADDR H22

58 — [MADR:H22] IMEM:RD3 → [3] TEST
H2Ø2Ø2Ø TO TEST WORD 3

59 — INV CJP :ERR6
TEST BIT 2 OF BYTE 1 WORD 3 FOR 1

[3] TSTBYT1 (2) =1?
TRUE
FALSE

5A — JUMP :WRTB
JUMP TO WRTB

WRTA 5B — [MADR:H22] ROM:RD2 → IMEM
Ø TO IMEM ADDR H22 (ROM ADDR H22=HØØØØ2Ø)

5C — [MADR:H22] IMEM:RD3 → [3] TEST
Ø TO TEST WORD 3

5D — CJP :ERR6A
TEST BIT2 OF BYTE1 WORD 3 FOR Ø

[3] TSTBYT1 (2) =1?
FALSE
TRUE

ERR 6 145 — JUMP TASKTERM: ERR 6
IF WRT3 DID NOT WRITE A 1 IN BIT 2, TASKTERM

ERR6A 146 — JUMP TASKTERM: ERR 6A
IF WRT 3 DID NOT WRITE AØ IN BIT 2, TASKTERM

READ BYTE 2 TEST → CHECK BYTE2 TO BYTE1 AND BYTE 2 TO BYTE3 DATA TRANSFERS

WRTB 5E — [MADR:HB] ROM:RD3 → IMEM
Ø TO IMEM ADDR HB (ROM ADDR HB=HØØ1ØØØ)

5F — [MADR:HB] ROM:RD2 → IMEM
HLØ1Ø1Ø TO IMEM ADDR HB

6Ø — [MADR:HB] IMEM → [4] TEST
H1Ø1Ø1Ø TO TEST WORD 4

(H) SH.9

TEST WRITE CTRL ROM BYTE 3, START READ CTRL ROM BYTE 2 TEST

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TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE — DWG NO. DS21E1065 — UNIT WT. — SHEET 8 OF 30 SHEETS

DS21E1065 B

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READ BYTE 1 TEST → CHECK BYTE 1 TO BYTE 2 AND BYTE 1 TO BYTE 3 DATA TRANSFERS

H (SH. 8)

61
INV CJP :ERR7
TEST BIT 3 OF BYTE 1 WORD 4 FOR 1

[4] TSTBYT1(3) =1?
TRUE
FALSE

62
[MADR:H8] IMEM:RD3 → [5] TEST
H101010 TO TEST WORD 5

63
INV CJP :ERR7A
TEST BIT 3 OF BYTE 1 WORD 5 FOR 1

[5] TSTBYT1(3) =1?
TRUE
FALSE

64
[MADR:4] ROM:RD3 → IMEM
Ø TO IMEM ADDR 4 (ROM ADDR 4 = HØ8ØØØØ)

65
[MADR:4] ROM:RD1 → IMEM
HØBØBØB TO IMEM ADDR 4

66
[MADR:4] IMEM → [6] TEST
HØBØBØ8 TO TEST WORD 6

ERR7 147
JUMP TASKTERM: ERR 7
IF BYTE 2-1 TRANSFER IN ERROR, TASKTERM

ERR7A 148
JUMP TASKTERM: ERR 7A
IF BYTE 2-3 TRANSFER IN ERROR, TASKTERM

WRITE BYTE 3 TEST → CHECK THE VALIDITY OF NOT WRITING TO BYTE 3

67
INV CJP :ERR8
TEST BIT 4 OF BYTE 2 WORD 6 FOR 1

[6] TSTBYT2(4) =1?
TRUE
FALSE

68
[MADR:4] IMEM:RD3 → [7] TEST
HØBØBØB TO TEST WORD 7

69
INV CJP :ERR8A
TEST BIT 4 OF BYTE 2 WORD 7 FOR 1

[7] TSTBYT2(4) =1?
TRUE
FALSE

6A
[MADR:H22] ROM:RD2 → IMEM
Ø TO IMEM ADDR H22 (ROM ADDR H22 = HØØØØ2Ø)

6B
[MADR:H22] ROM → IMEM:WRTØ
WRTØ → WRITE NO BYTES, SO THIS IS A NOP

(I) SH. 1Ø

ERR8 149
JUMP TASKTERM: ERR8
IF BYTE 1-2 TRANSFER IN ERROR, TASKTERM

ERR8A 14A
JUMP TASKTERM: ERR8A
IF BYTE 1-3 TRANSFER IN ERROR, TASKTERM

FINISH READ CTRL ROM BYTE 2 TEST,
TEST READ CTRL ROM BYTE 1,
START ADDITIONAL WRITE CTRL
ROM BYTE 3 TEST

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TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: X
DWG NO. DS21E1065
UNIT WT. X
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ALU TEST → FIRST LOAD THE REGISTER FILES

(I) SH.9

6C [MADR:HZZ][IMEM:RD3] → [B] TEST
Ø TO TEST WORD B

6D Ø → Q; CJP :ERR6B
TEST BIT 2 OF BYTE 1 WORD B FOR Ø, LOAD Ø TO Q REG

[B] TSTBYT1 (2) =1?
FALSE
TRUE

6E Ø → RØ
Ø TO RØ

6F 1+RØ → R1
1 TO R1

7Ø R1,LS → R2
2 TO R2

71 R2,LS → R3
4 TO R3

ERR6B 14B
JUMP TASKTERM:ERR6B
IF WRTØ DID NOT INHIBIT WRITING TO BYTE 3, TASKTERM

72 R3,LS → R4
8 TO R4

73 R4,LS → R5
H1Ø TO R5

74 R5,LS → R6
H2Ø TO R6

75 R6,LS → R7
H4Ø TO R7

76 R7,LS → R8
H8Ø TO R8

77 R8,LS → R9
H1ØØ TO R9

78 R9,LS → R1Ø
H2ØØ TO R1Ø

79 R1Ø,LS → R11
H4ØØ TO R11

7A R11,LS → R12
H8ØØ TO R12

7B R12,LS → R13
H1ØØØ TO R13

7C R13,LS → R14
H2ØØØ TO R14

7D R14,LS → R15; LDCOND
H4ØØØ TO R15, LATCH THE F=Ø CONDITION FALSE

(J) SH.11

FINISH WRITE CTRL ROM BYTE 3 TEST, START ALU TEST

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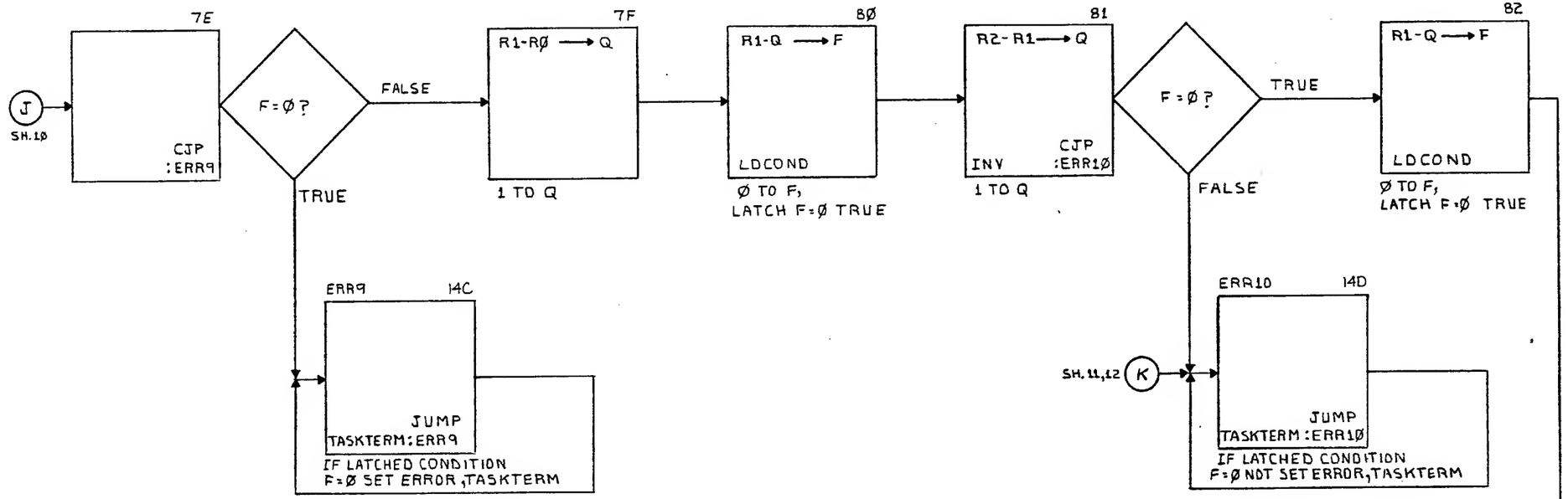
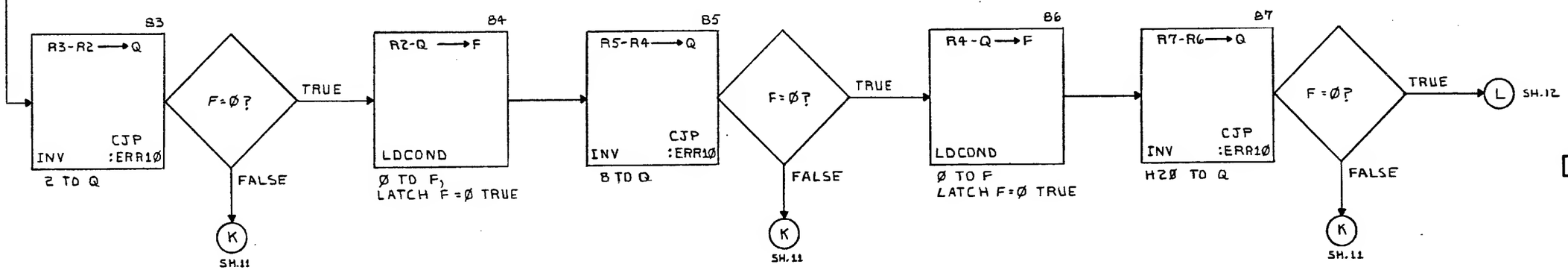
TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: X
DWG NO. DS21E1065
UNIT WT. X
SHEET 10 OF 30 SHEETS

MAKEPEACE P-3095

ALU TEST → NOW USE THE REGISTER FILE, Q REG, AND ARITHMETIC SECTION TO CHECK THE ALU OPERATION





CONTINUE ALU TEST,
CHECK F=Ø LATCHED CONDITION

DS21E1065
B

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FINISH: X
PART NUMBER | NEXT ASSEMBLY | QTY

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TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

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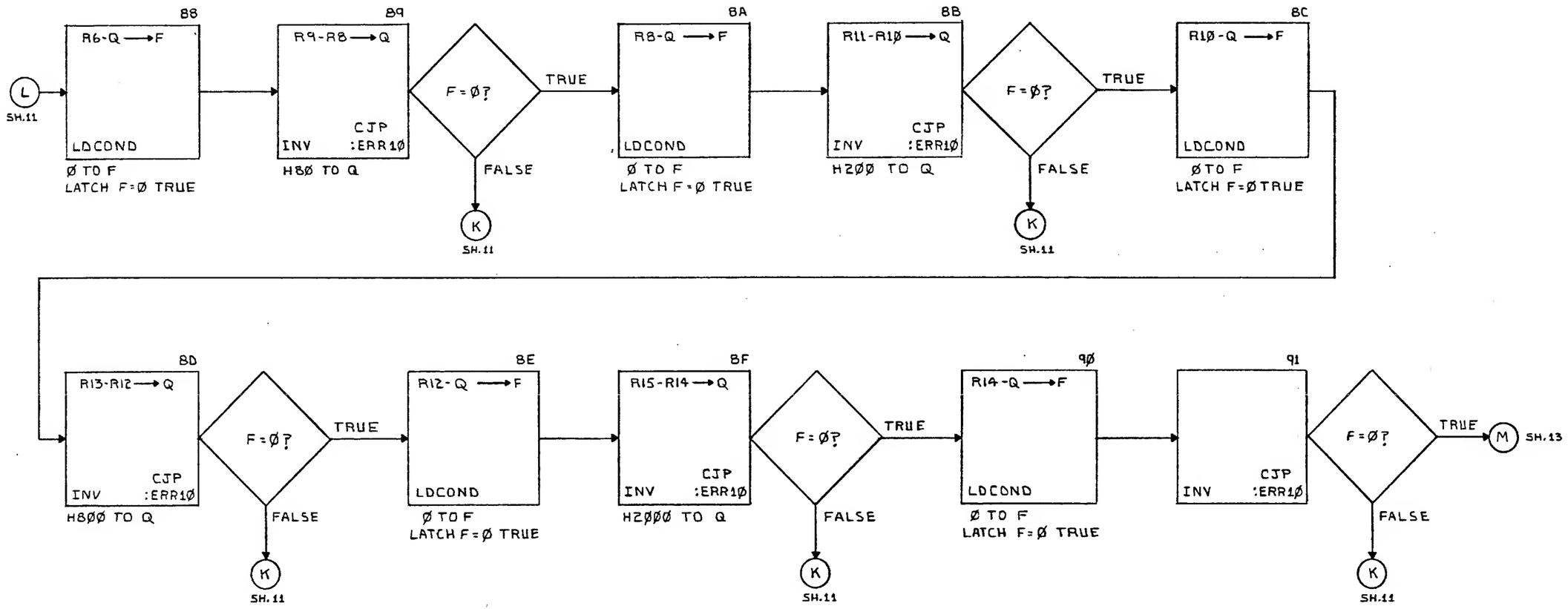
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: GPU MICROPROGRAM FLOW CHARTS
SCALE: X
DWG NO. DS21E1065
UNIT WT. X
SHEET 11 OF 30 SHEETS

MAKEPEACE P-2059



DS21E1065

B

FINISH ALU ARITHMETIC TEST

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FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

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SYM	REVISION DESCRIPTION	APPD	DATE

TITLE
GPU MICROPROGRAM FLOW CHARTS

SCALE
DWG NO. DS21E1065
UNIT WT.
SHEET 12 OF 30 SHEETS

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CHECK FBYT2 =Ø AND FBYT3 =Ø →

ROM TO IBUS TO ALU TESTS → CHECK F3 AND OVR1 LATCHED CONDITIONS

M SH.12

92
R9 → F
LDCOND
HIØØ TO F,
LATCH FBYT2 =Ø FALSE

93
CJP :ERR1ØA

FBYT2 =Ø ?
FALSE
TRUE

94
R2 → F
LDCOND
2 TO F,
LATCH FBYT3 =Ø FALSE

95
CJP :ERR1ØB

FBYT3 =Ø ?
FALSE
TRUE

96
IB .EXOR. R11 → F
[MADR:HQ] ROM → IB
LD COND
H4ØØ TO IB,
Ø TO F,
LATCH F=Ø TRUE

ERR1ØA 14E
JUMP TASKTERM:ERR1ØA
IF FBYT2 =Ø SET IN ERROR, TASKTERM

ERR1ØB 14F
JUMP TASKTERM:ERR1ØB
IF FBYT3 =Ø SET IN ERROR, TASKTERM

97
IB.EXOR. Ø → F
[MADR:Ø] ROM → IB
INV CJP
LDCOND :ERR1ØC
H8ØØØØØ TO IB,
HF8ØØØØØ TO F
LATCH F3=1 TRUE
(THE 4 MSB'S OF F ARE THE OVERFLOW SLICE)

F=Ø ?
FALSE
TRUE

98
IB, LS → R12
[MADR:2] ROM → IB
INV CJP :ERR11
H2ØØØØØ TO IB,
H4ØØØØØ TO R12

F3=1 ?
FALSE
TRUE

99
IB +R12 → F
[MADR:1] ROM → IB
LDCOND
H4ØØØØØ TO IB,
HØ8ØØØØØ TO F,
LATCH OVR1=1 TRUE,
LATCH F3=1 FALSE

9A
INV CJP :ERR12

OVR1 =1 ?
FALSE
TRUE
N SH.14

ERR1ØC 150
JUMP TASKTERM:ERR1ØC
IF ROM TO IB TO ALU IN ERROR, TASKTERM

ERR11 151
JUMP TASKTERM :ERR11
IF F3 DID NOT GET SET, TASKTERM

ERR12 152
JUMP TASKTERM :ERR12
IF OVR1 DID NOT GET SET, TASKTERM

CHECK FBYT2 =Ø AND FBYT3 =Ø LATCH COND, CHECK F3 AND OVR1 LATCH COND BY USING ROM TO IBUS TO ALU DATA PATH

DS21E1065 B

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.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
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SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU MICROPROGRAM FLOW CHARTS

SCALE — DWG NO. DS21E1065
UNIT WT. — SHEET 13 OF 30 SHEETS

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ALU OUTPUT TO IBUS TEST

9B: Ø → F
CJP :ERR11A
LDCOND
Ø TO F, LATCH OVR1=1 FALSE

N SH.13

F3=1 ? — TRUE

9C: CJP :ERR12A

OVR1=1 ? — TRUE

9D: IB → RIØ
[MADR:H2B] ROM → IB
HAAAAAA TO RIØ

9E: RIØ → F
[F] ALU → [MADR:Ø] IMEM
HAAAAAA TO IMEM ADDR Ø

9F: IB.EXOR.RIØ → F
[MADR:Ø] IMEM → IB
LDCOND
HAAAAAA TO IB, Ø TO F, LATCH F=Ø TRUE

ERR11A 153: JUMP TASKTERM:ERR11A
IF F3 REMAINED SET, TASKTERM

ERR12A 154: JUMP TASKTERM:ERR12A
IF OVR1 REMAINED SET, TASKTERM

BYPASS ALU TO IBUS TEST →

AØ: INV CJP :ERR13

F=Ø ? — TRUE

A1: [R12] ALU → [HF] TEST
HØØØØØØ TO TEST WORD F

A2: INV CJP :ERR14
TEST BIT 1 OF BYTE1 WORD F FOR 1

[HF] TSTBY T1 (1) = 1 ? — TRUE

Q REG LEFT SHIFT →

A3: IB → Q
[MADR:H7D] ROM → IB
FLAG(7)=1
HD55555 TO Q, SET FLAG 7

A4: Q,LS FLAG(7) → Q
LEFT SHIFT Q AND NOT TB7 SHIFTED INTO THE LSB OF Q, HENCE Q=HAAAAAA

A5: IB.EXOR.Q → F
[MADR:H2B] ROM → IB
LDCOND
HAAAAAA TO IBUS, Ø TO F, LATCH F=Ø TRUE

O SH.15

FALSE

ERR13 155: JUMP TASKTERM:ERR13
IF ALU OUTPUT TO IBUS IN ERROR, TASKTERM

ERR 14 156: JUMP TASKTERM :ERR 14
IF REG TO IBUS IN ERROR, TASKTERM

CHECK ALU OUTPUT TO IBUS,
CHECK REG FILE ALU BYPASS TO IBUS,
START TEST OF Q REG LEFT SHIFT

D521E1065 B

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MATERIAL · FINISH · PART NUMBER · NEXT ASSEMBLY · QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 30'

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PROJ
MFG
SIGNATURE DATE

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SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE · DWG NO. D521E1065 · UNIT WT. · SHEET 14 OF 30 SHEETS

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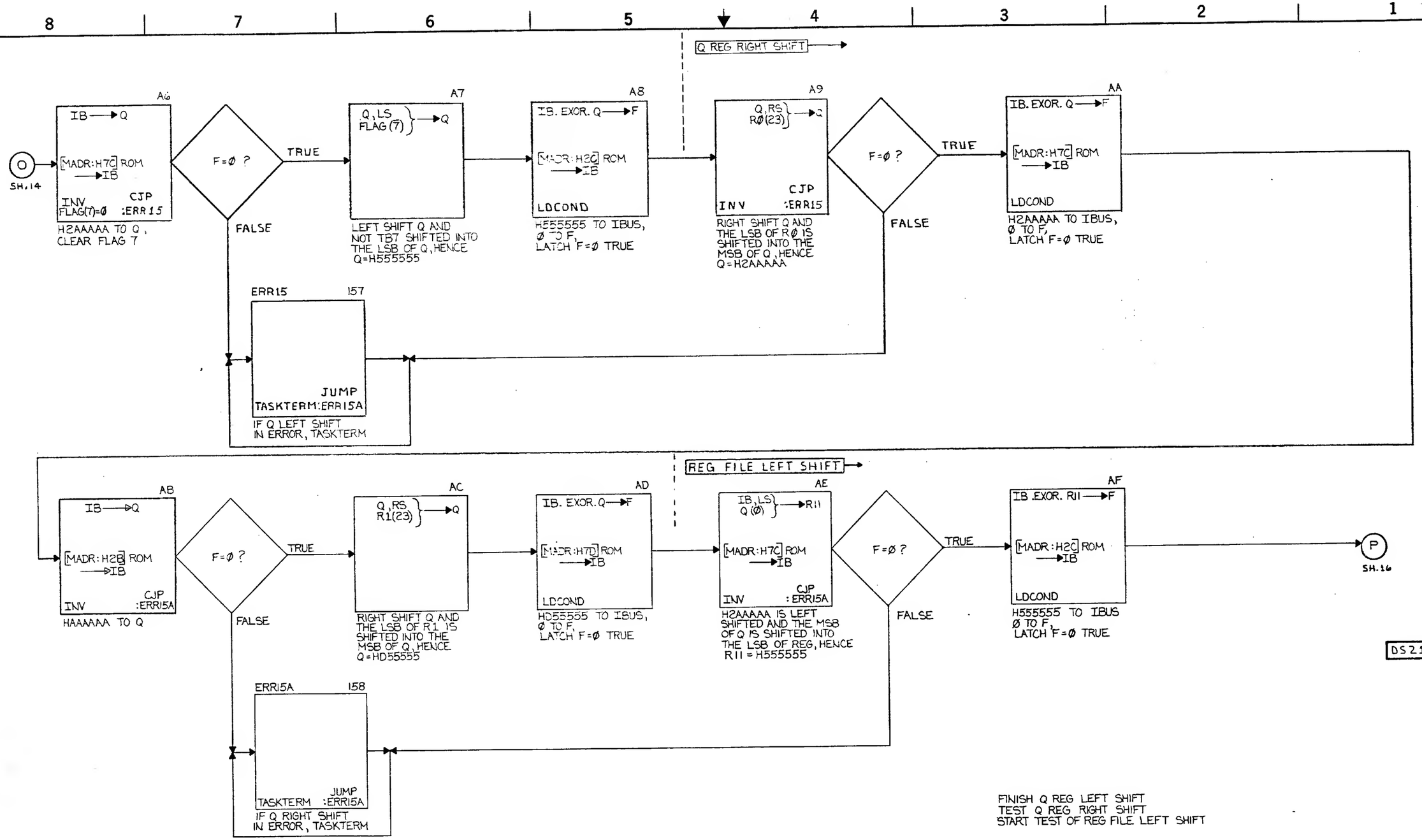

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TOLERANCES						
DECIMAL						
.XX ±.01						
.XXX ±.005						
.XXXX ±.0010						
FRACTIONAL ± 1/64						
ANGULAR ± 1°00'						
MATERIAL						
x						
FINISH						
x						
PART NUMBER	NEXT ASSEMBLY	QTY				
DRN D.O'Hearn 10-7						
CHK						
ENGR						
PROJ						
MFG						
SIGNATURE DATE						
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SYM	REVISION DESCRIPTION				APPD	DATE

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TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: x | DWG NO. DS21E1065 | UNIT WT. x | SHEET 15 OF 30 SHEETS

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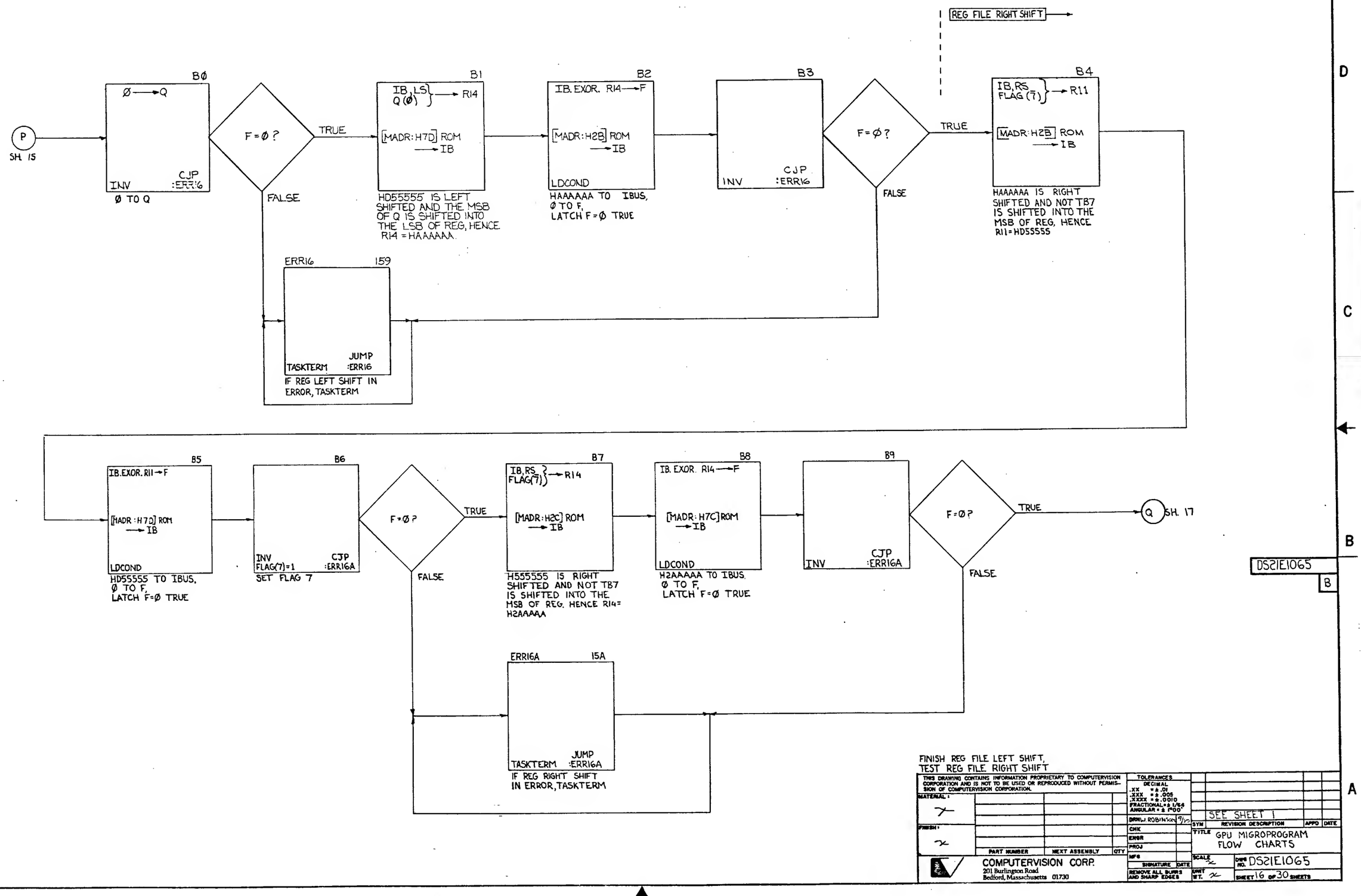

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TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± .5 DEG

MATERIAL: X
FINISH: X

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PART NUMBER	NEXT ASSEMBLY	QTY

SIGNATURE DATE

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SYM	REVISION DESCRIPTION	APPD	DATE
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TITLE: GPU MIGROPROGRAM FLOW CHARTS

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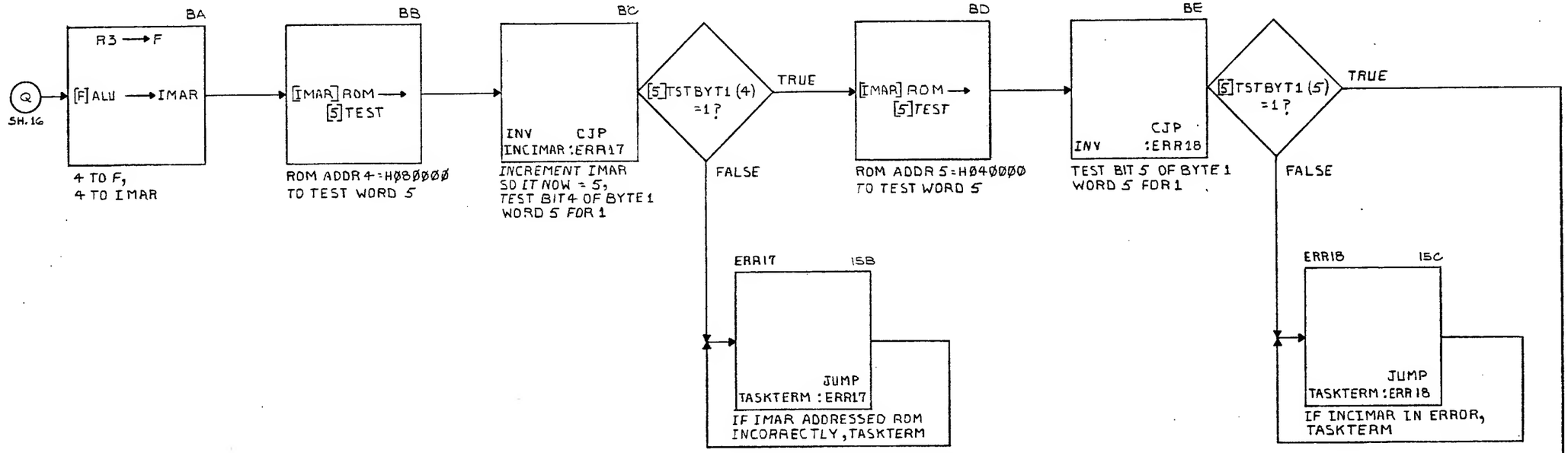
SCALE X
DWG NO. DS21E1065
UNIT WT. X
SHEET 16 OF 30 SHEETS

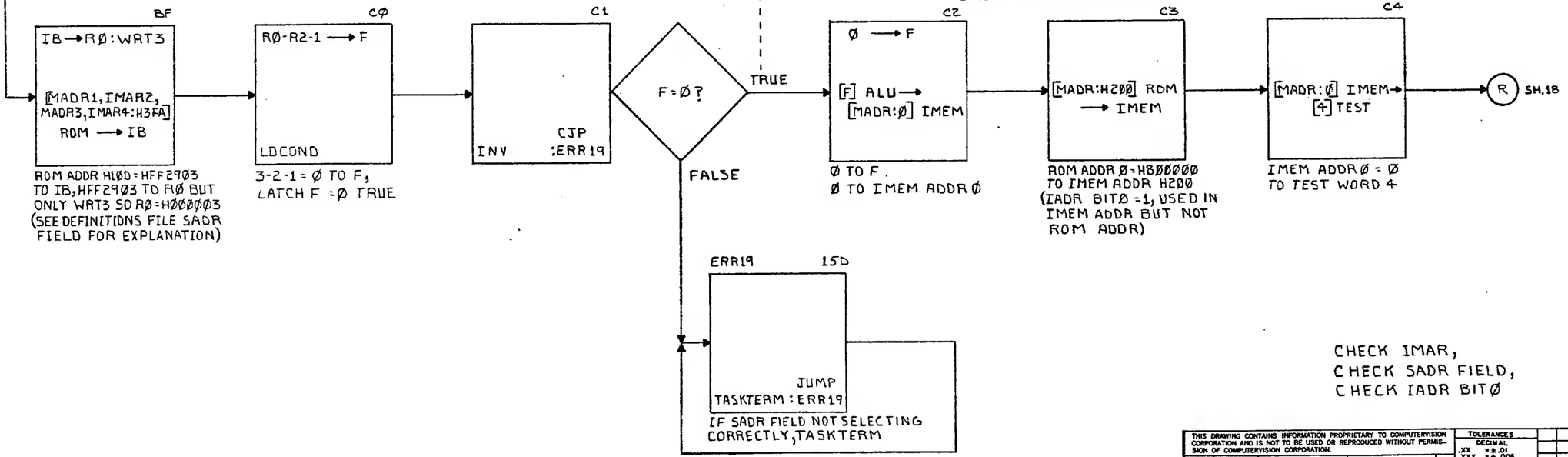
DS21E1065
B

SHAKEPROOF P-3747

IMAR AND SADR TEST → LOAD THE IMAR AND ADDRESS THE ROM FROM IT,
USING THE SADR FIELD SELECT A MADR-IMAR COMBINATION TO ADDRESS THE ROM



IADR BIT Ø TEST → CHECK TO INSURE IT IS ADDRESSING
IMEM BUT NOT ROM



CHECK IMAR,
CHECK SADR FIELD,
CHECK IADR BITØ

DS21E1065
B

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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL: X
FINISH: X

PART NUMBER | NEXT ASSEMBLY | QTY

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REMOVE ALL BURRS AND SHARP EDGES

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SYM	REVISION DESCRIPTION	CK	APPD	DATE

TITLE: GPU MICROPROGRAM FLOW CHARTS

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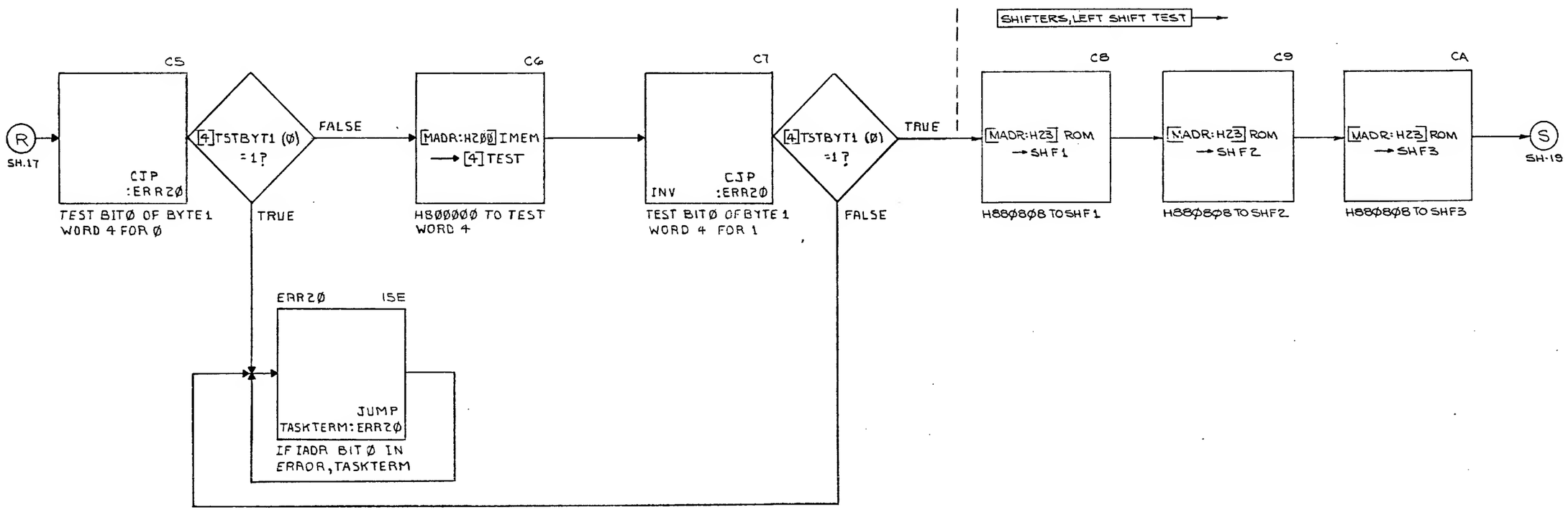
SCALE: X
UNIT WT.: X
DWG NO. DS21E1065
SHEET 17 OF 30 SHEETS

MAKEPEACE P-2098



FINISH IADR BIT Ø TEST
START SHIFTER LEFT SHIFT TEST

DS21E1065
B

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TOLERANCES						
DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ± 1/64 ANGULAR ± 2 PLACE DECIMAL						
MATERIAL ~						
FINISH ~						
PART NUMBER	NEXT ASSEMBLY	QTY				
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CHK				SEE SHEET 1		
ENGR			TITLE	GPU MICROPROGRAM FLOW CHARTS		
PROJ						
MFG			SCALE ~	DWG NO. DS21E1065		
SIGNATURE DATE			UNIT WT. ~	SHEET 18 OF 30 SHEETS		

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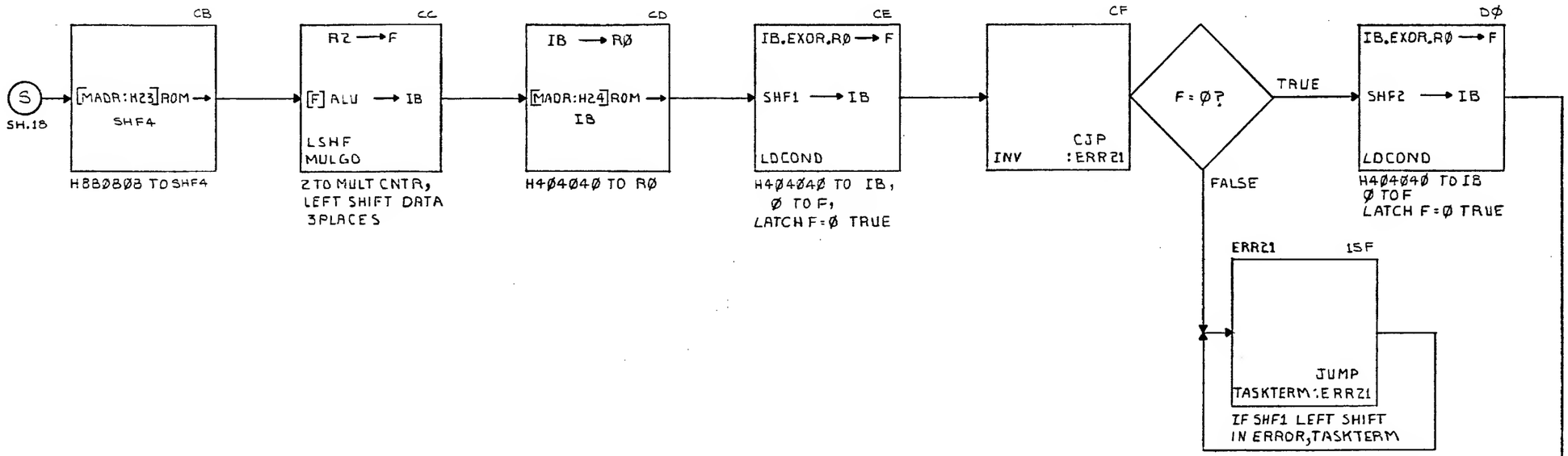

DS21E1065
B

TEST SHIFTERS, *LEFT SHIFT*

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TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 8 MIN

MATERIAL *
FINISH *
DRN D.O'Hearn 10-7-8
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MFG
SIGNATURE DATE
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PART NUMBER | NEXT ASSEMBLY | QTY

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SYM	REVISION DESCRIPTION	APPD	DATE

TITLE
GPU MICROPROGRAM
FLOW CHARTS

SCALE ~
DWG NO. DS21E1065
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SHEET 13 OF 30 SHEETS

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SHIFTERS, RIGHT SHIFT TEST →

D6

T
SH.19

[MADR:H23] ROM
SHF1,SHF2,SHF3,SHF4

H880808 TO ALL
4 SHIFTERS

D7

R3 → F

[F] ALU → IB

RSSEX
MULGD

4 TO MULT CNTR,
RIGHT SHIFT DATA
WITH SIGN EXTEND
5 PLACES

D8

IB → RØ

[MADR:H25] ROM → IB

HFC4040 TO RØ

D9

IB.EXOR.RØ → F

SHF1 → IB

LDCOND

HFC4040 TO IB,
Ø TO F,
LATCH F=Ø TRUE

DA

INV CJP :ERR25

F=Ø?

TRUE

FALSE

DB

IB.EXOR.RØ → F

SHF2 → IB

LDCOND

HFC4040 TO IB,
Ø TO F,
LATCH F=Ø TRUE

ERR25 163

JUMP
TASKTERM:ERR25

IF SHF1 RIGHT SHIFT
IN ERROR, TASKTERM

DC

INV CJP :ERR26

F=Ø?

TRUE

FALSE

DD

IB.EXOR.RØ → F

SHF3 → IB

LDCOND

HFC4040 TO IB
Ø TO F
LATCH F=Ø TRUE

DE

INV CJP :ERR27

F=Ø?

TRUE

FALSE

DF

IB.EXOR.RØ → F

SHF4 → IB

LDCOND

HFC4040 TO IB
ØTO F
LATCH F=Ø TRUE

EØ

INV CJP :ERR28

F=Ø?

TRUE

U SH.21

FALSE

ERR26 164

JUMP
TASKTERM:ERR26

IF SHF2 RIGHT SHIFT
IN ERROR, TASKTERM

ERR27 165

JUMP
TASKTERM:ERR27

IF SHF3 RIGHT SHIFT
IN ERROR, TASKTERM

ERR28 166

JUMP
TASKTERM:ERR28

IF SHF4 RIGHT SHIFT
IN ERROR, TASKTERM

TEST SHIFTERS, RIGHT SHIFT
WITH SIGN EXTEND

DS21E1065
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.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL +
FINISH +

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SYM	REVISION DESCRIPTION	APPD	DATE

TITLE
GPU MICROPROGRAM
FLOW CHARTS

SCALE +
DWG NO. DS21E1065
UNIT WT. +
SHEET 23 OF 30 SHEETS

MAKEPEACE P-2059

SHIFTER/MULTIPLIER TEST →

E1 — [MADR:H21] ROM → SHF1,SHF2,SHF3,SHF4
H8Ø4ØØØ TO ALL 4 SHIFTERS

E2 — [MADR:H24] ROM → IMEM
H4Ø4Ø4Ø TO IMEM ADDR H24

E3 — IB → RØ; [MADR:H26] ROM → IB
HBFDFEØ TO RØ

E4 — [MADR:H24] IMEM → MUL1
H4Ø4Ø4Ø TO MUL1

E5 — [MADR:H24] IMEM → MUL2
H4Ø4Ø4Ø TO MUL2

E6 — [MADR:H24] IMEM → MUL3
H4Ø4Ø4Ø TO MUL3

E7 — [MADR:H24] IMEM → MUL4
H4Ø4Ø4Ø TO MUL4

(U) SH.2Ø

E8 — [MADR:H27] ROM → IB; MULT; MULGO
48 TO MULT COUNTER
MULTIPLY H8Ø4ØØØ TIMES H4Ø4Ø4Ø USING 49 MULT CYCLES

E9 — IB.EXOR.RØ → F; SHF1 → IB; LDCOND
HBFDFEØ TO IB, Ø TO F, LATCH F=Ø TRUE

EA — INV; CJP :ERR29
F=Ø? TRUE

EB — IB.EXOR.RØ → F; SHF2 → IB; LDCOND
HBFDFEØ TO IB Ø TO F, LATCH F=Ø TRUE

EC — INV; CJP :ERR30
F=Ø? TRUE

ED — IB.EXOR.RØ → F; SHF3 → IB; LDCOND
HBFDFEØ TO IB Ø TO F, LATCH F=Ø TRUE

FALSE

ERR29 167 — JUMP TASKTERM: ERR29
IF SHF1/MUL1 LOGIC IN ERROR, TASKTERM

ERR30 168 — JUMP TASKTERM: ERR3Ø
IF SHF2/MUL2 LOGIC IN ERROR, TASKTERM

EE — INV; CJP :ERR31
F=Ø? TRUE

ERR31 169 — JUMP TASKTERM: ERR31
IF SHF3/MUL3 LOGIC IN ERROR, TASKTERM

EF — IB.EXOR.RØ → F; SHF4 → IB; LDCOND
HBFDFEØ TO IB, Ø TO F, LATCH F=Ø TRUE

FØ — INV; CJP :ERR32
F=Ø? TRUE

ERR32 16A — JUMP TASKTERM: ERR32
IF SHF4/MUL4 LOGIC IN ERROR, TASKTERM

(V) SH.22

TEST SHIFTER / MULTIPLIER LOGIC

DS21E1065 B

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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

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ENGR
PROJ
MFG
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SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: X
UNIT WT.: X
DWG NO. DS21E1065
SHEET 21 OF 30 SHEETS

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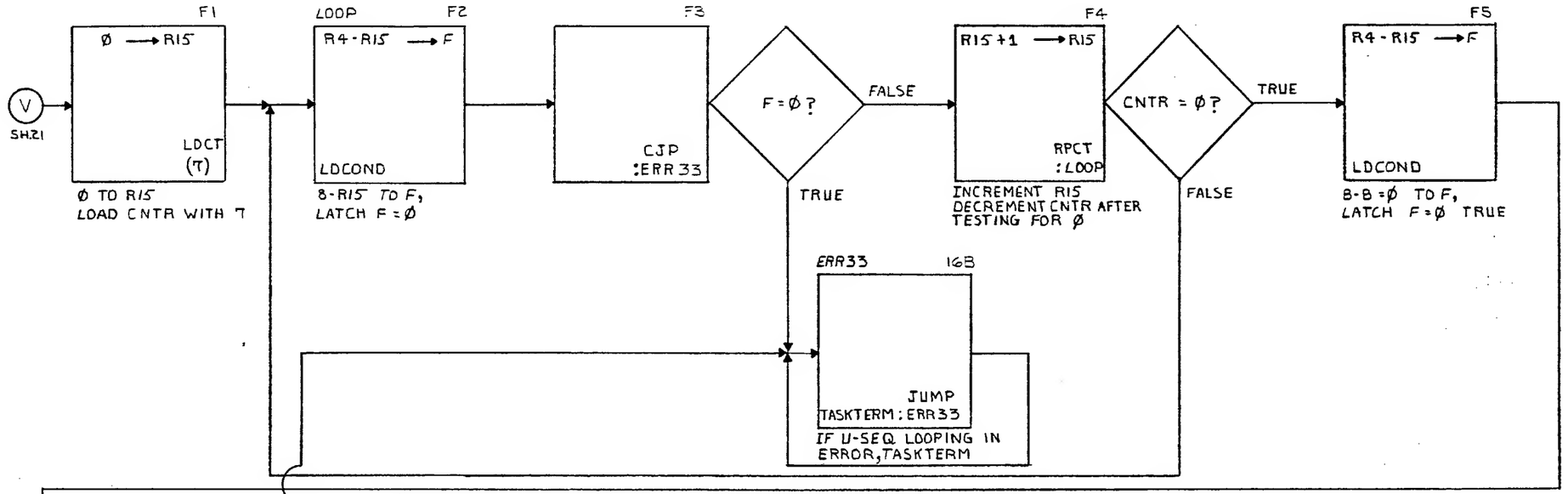
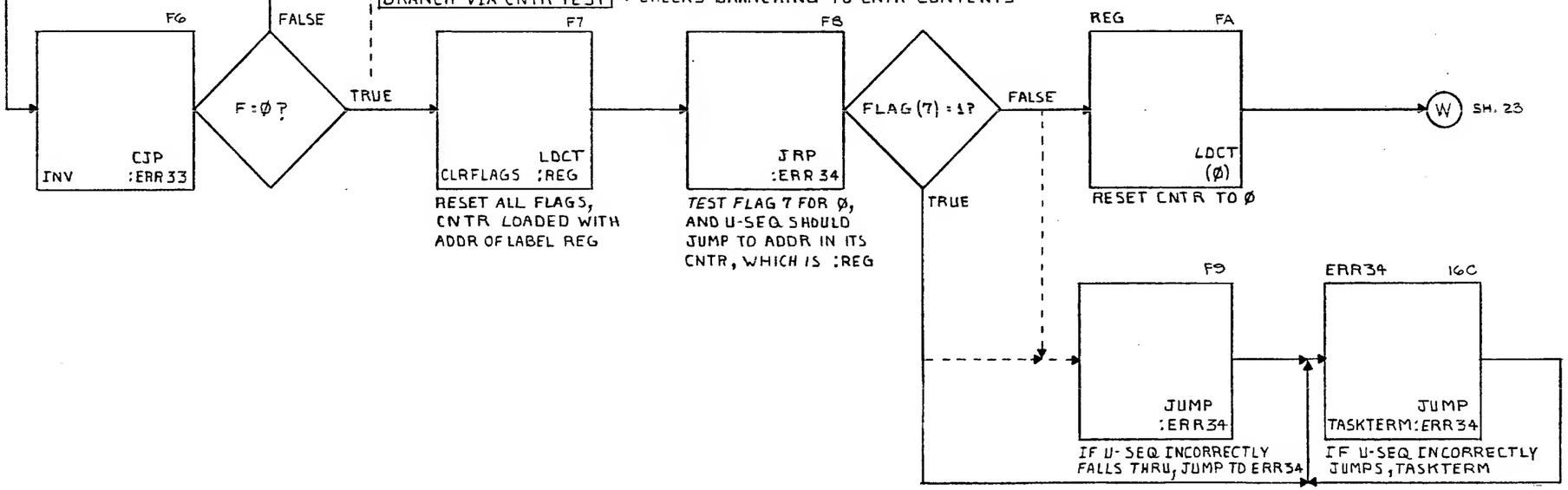
MAKEPEACE P-2059

U-SEQ LOOPING TEST → CHECKS BRANCHING ON CNTR CONTENTS



BRANCH VIA CNTR TEST → CHECKS BRANCHING TO CNTR CONTENTS



TEST U-SEQ LOOPING;
TEST U-SEQ BRANCH
VIA CNTR CONTENTS

DS21E1065
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FINISH: X
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

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PROJ
MFG
SIGNATURE DATE

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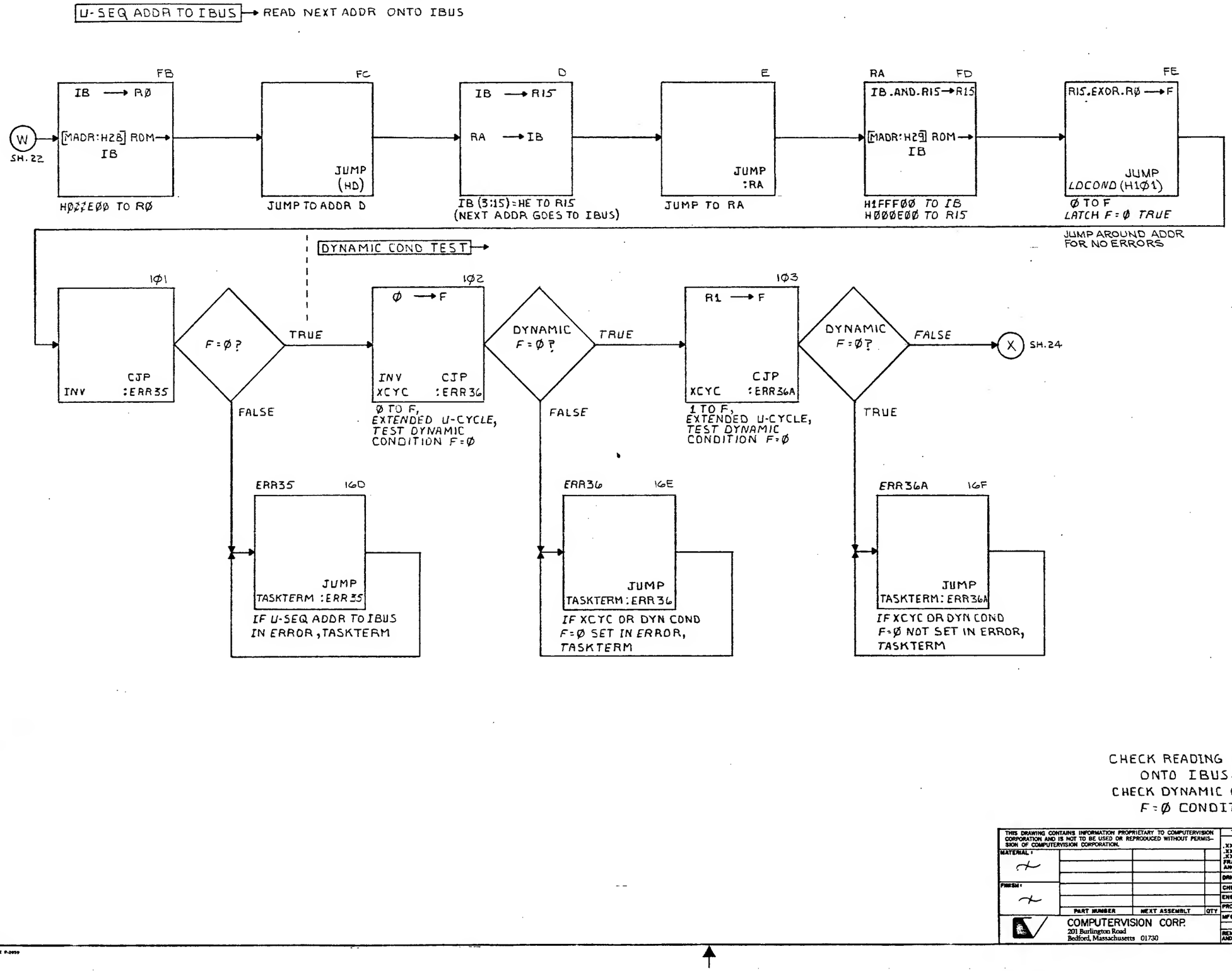
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: X
DWG NO. DS21E1065
UNIT WT. X
SHEET 22 OF 30 SHEETS

MAKEPEACE P-2099



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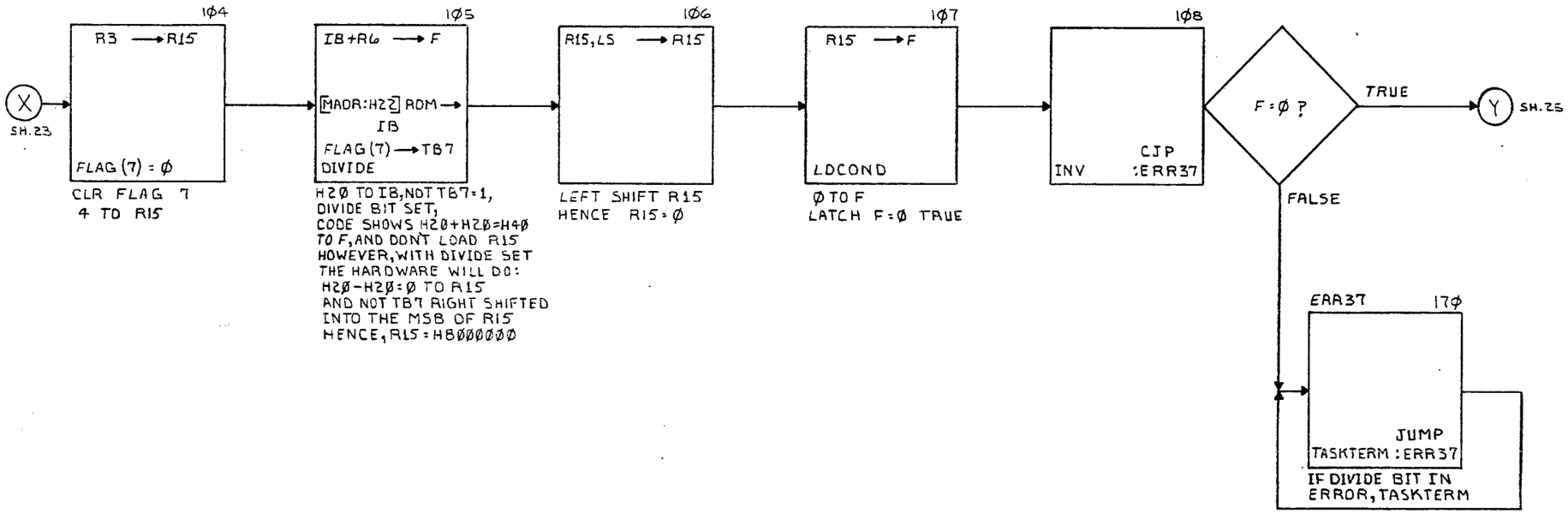
DIVIDE BIT TEST → CHECK TO INSURE THAT THE DIVIDE BIT ALTERS THE FUNCTION OF THE ALU



CHECK DIVIDE BIT

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B

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TOLERANCES					
DECIMAL					
.XX ±.01					
.XXX ±.005					
.XXXX ±.0010					
FRACTIONAL ± 1/64					
ANGULAR ± 5 MOD					
MATERIAL					
FINISH					
PART NUMBER	NEXT ASSEMBLY	QTY			
SIGNATURE	DATE				
REMOVE ALL BURRS AND SHARP EDGES					

DRN D.O'Heavn 10-79
CHK
ENGR
PROJ
MFG

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: -
DWG NO. DS21E1065
UNIT WT. -
SHEET 24 OF 30 SHEETS

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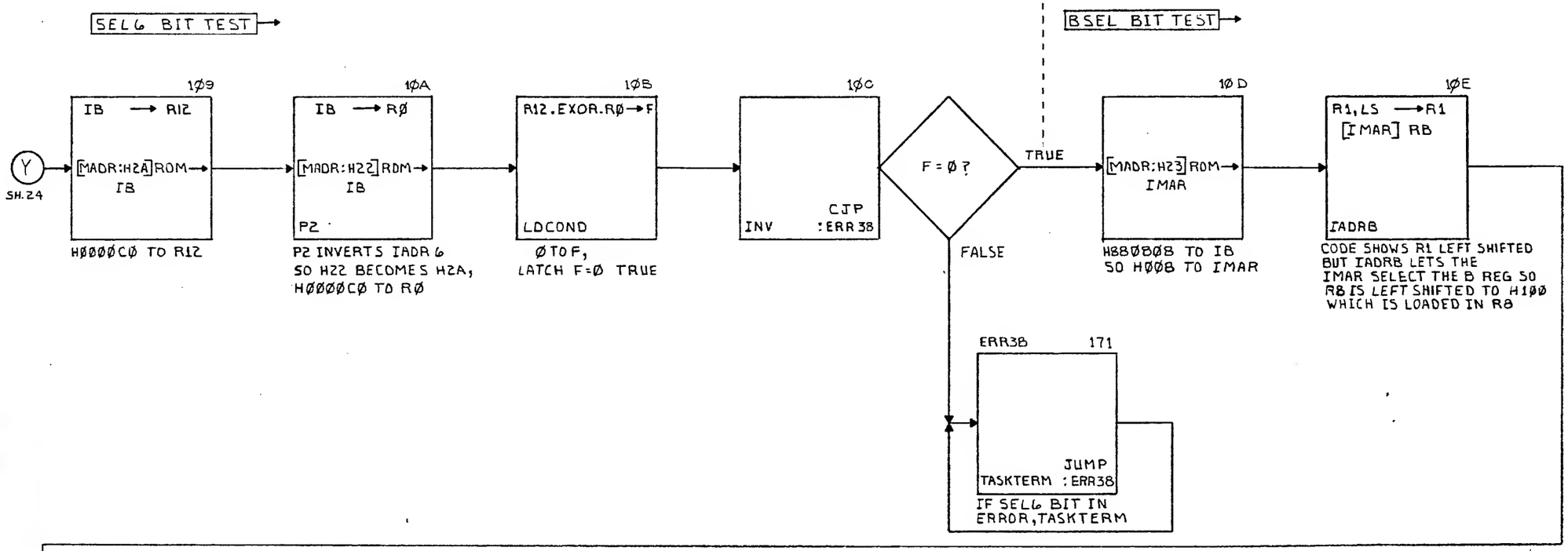
Bedford, Massachusetts 01730



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B

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MATERIAL: —
FINISH: —

PART NUMBER	NEXT ASSEMBLY	QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN D. O'Hearn 10-79
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: GPU MICROPROGRAM FLOW CHARTS

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SCALE —
DWG NO. DS21E1065
UNIT WT. —
SHEET 25 OF 30 SHEETS

MARKPLACE P-3059

IMEM TEST → TEST THE IMEM BY WRITING EACH ADDRESS WITH DATA EQUAL TO ITS OWN ADDRESS

111
Z
SH.25
Ø → RØ
Ø → IMAR
LDCT (H2FC)
Ø TO RØ AND IMAR, LOAD CNTR WITH A COUNT OF 2FC

IM1 112
RØ → F
[F] ALU → [IMAR] IMEM
RØ TO THE IMEM ADDRESS EQUAL TO THE IMAR

113
RØ+1 → RØ
INCIMAR
RPCT :IM1
INCREMENT RØ AND THE IMAR

CNTR = Ø?
TRUE
FALSE

114
Ø → RØ
Ø → IMAR
LDCT (H2FC)
Ø TO RØ AND IMAR, LOAD CNTR WITH A COUNT OF 2FC

IM2 115
IB → R15
[IMAR] IMEM → IB
THE IMEM ADDR EQUAL TO THE IMAR IS LOADED IN R15

116
RØ .EXOR. R15 → F
INV XCYC
CJP :ERR4Ø
COMPARE RØ TO R15

DYNAMIC F = Ø?
FALSE
TRUE

ERR4Ø 173
JUMP TASKTERM :ERR4Ø
IF IMEM DATA OR ADDRESSING ERROR, TASKTERM

BPORT TEST → TESTS THE BPORT LOGIC INCLUDING THE INFIFO AND THE CAR AND ALSO THE BMEMORY ITSELF

117
RØ+1 → RØ
INCIMAR
RPCT :IM2
INCREMENT RØ AND THE IMAR

CNTR = Ø?
FALSE
TRUE

BP1 118
Ø → R1
INV CLRFLAGS
CJP :BP13
Ø TO R1, CLEAR FLAGS, TEST BIT 1 OF BYTE 1 WORD Ø FOR 1

[Ø]TSTBYT1 (1) = 1?
TRUE
FALSE

BB
SH.3Ø

GG
SH.29

BP2 119
IB → RØ
[MADR:H2FE] IMEM → IB
LDCT :BP6
BMEM START ADDR TO RØ

11A
IB-RØ → R15
[MADR:H2FF] IMEM → IB
BMEM END ADDR - BMEM START ADDR TO R15

AA
SH.27

TEST IMEM; CHECK FOR BPORT TEST

DS21E1065
B

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TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL: X
FINISH: X
PART NUMBER | NEXT ASSEMBLY | QTY

DRN J. O'Meara 10-79
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	APPD	DATE
A	SEE SHEET 1		

TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: X
DWG NO. DS21E1065
UNIT WT. X
SHEET 26 OF 30 SHEETS

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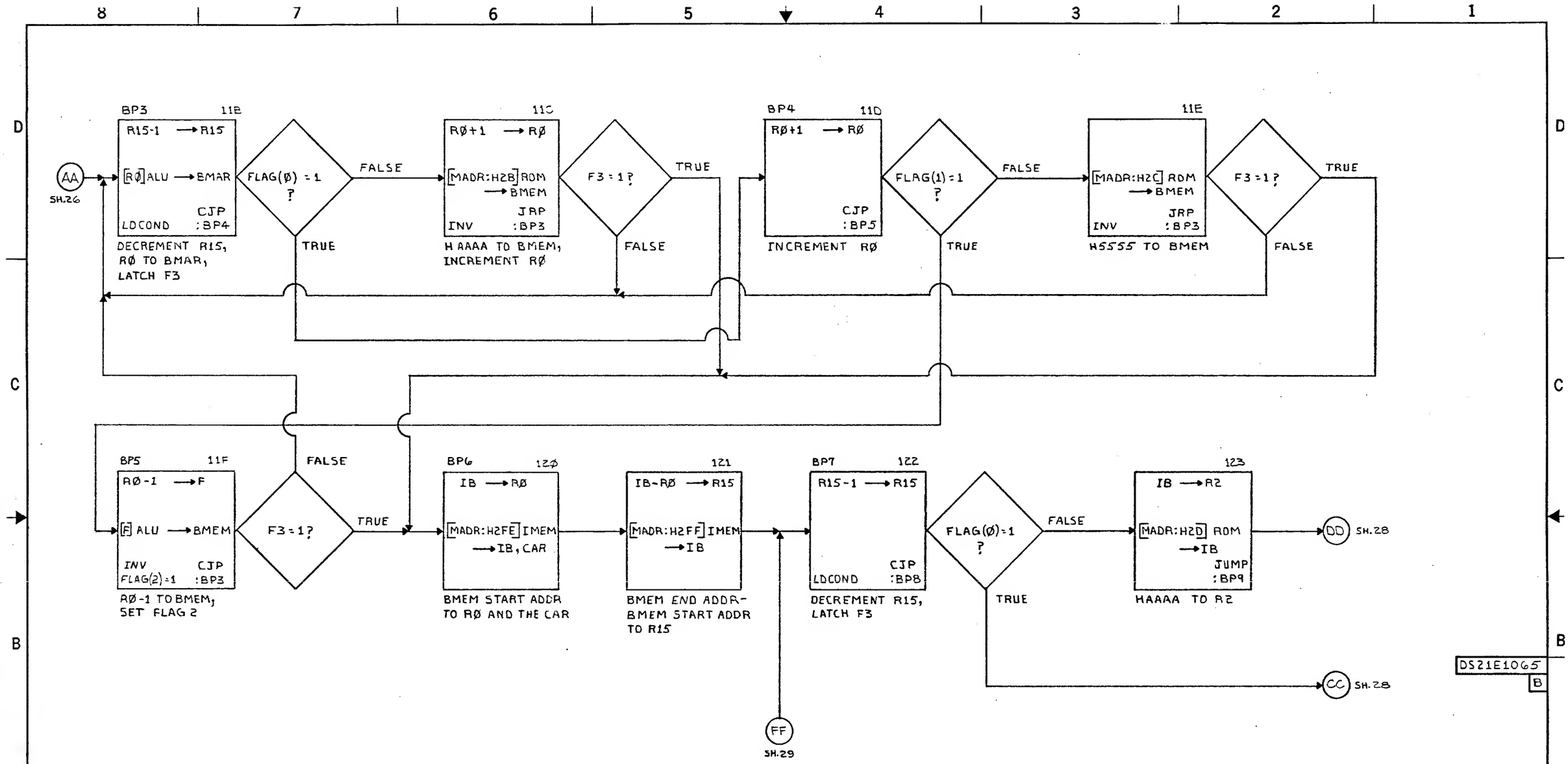

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B

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TOLERANCES					
DECIMAL					
.XX ± .01					
.XXX ± .005					
.XXXX ± .0010					
FRACTIONAL ± 1/64					
ANGULAR ± 1°00'					
DRN D. O'Hearn 10-77					
CHK					
ENGR					
PROJ					
MFG					
SIGNATURE DATE					
REMOVE ALL BURRS AND SHARP EDGES					

MATERIAL	PART NUMBER	NEXT ASSEMBLY	QTY
~			
FINISH ~			

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHEET 1		

TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: ~ | DWG NO. DS21E1065 | UNIT WT. ~ | SHEET 27 OF 30 SHEETS

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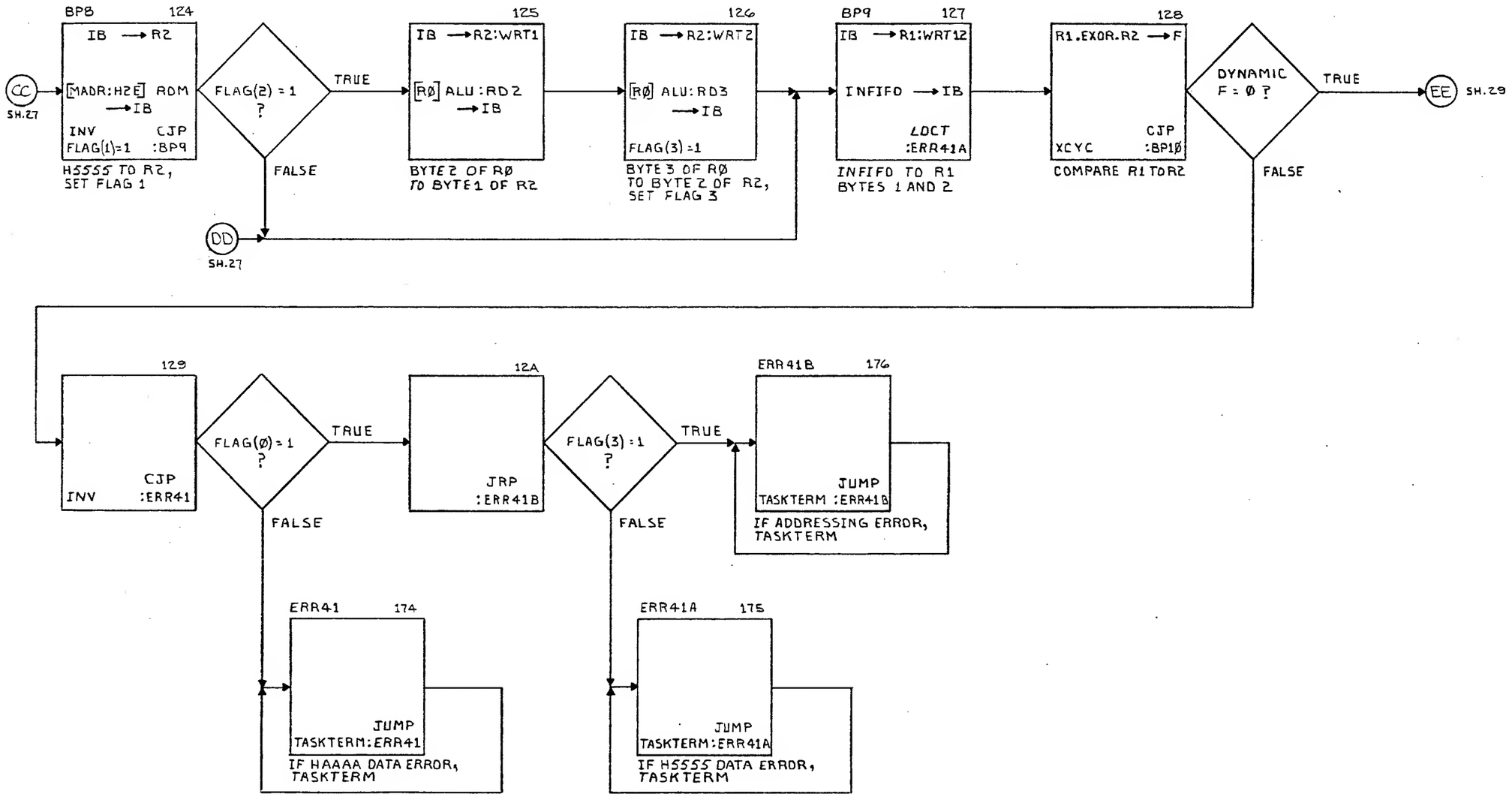

CONTINUE BPORT TEST

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B

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TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL: *
FINISH: *
DRN D. O'Hearn 10-7-
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ENGR
PROJ
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PART NUMBER NEXT ASSEMBLY QTY
SIGNATURE DATE
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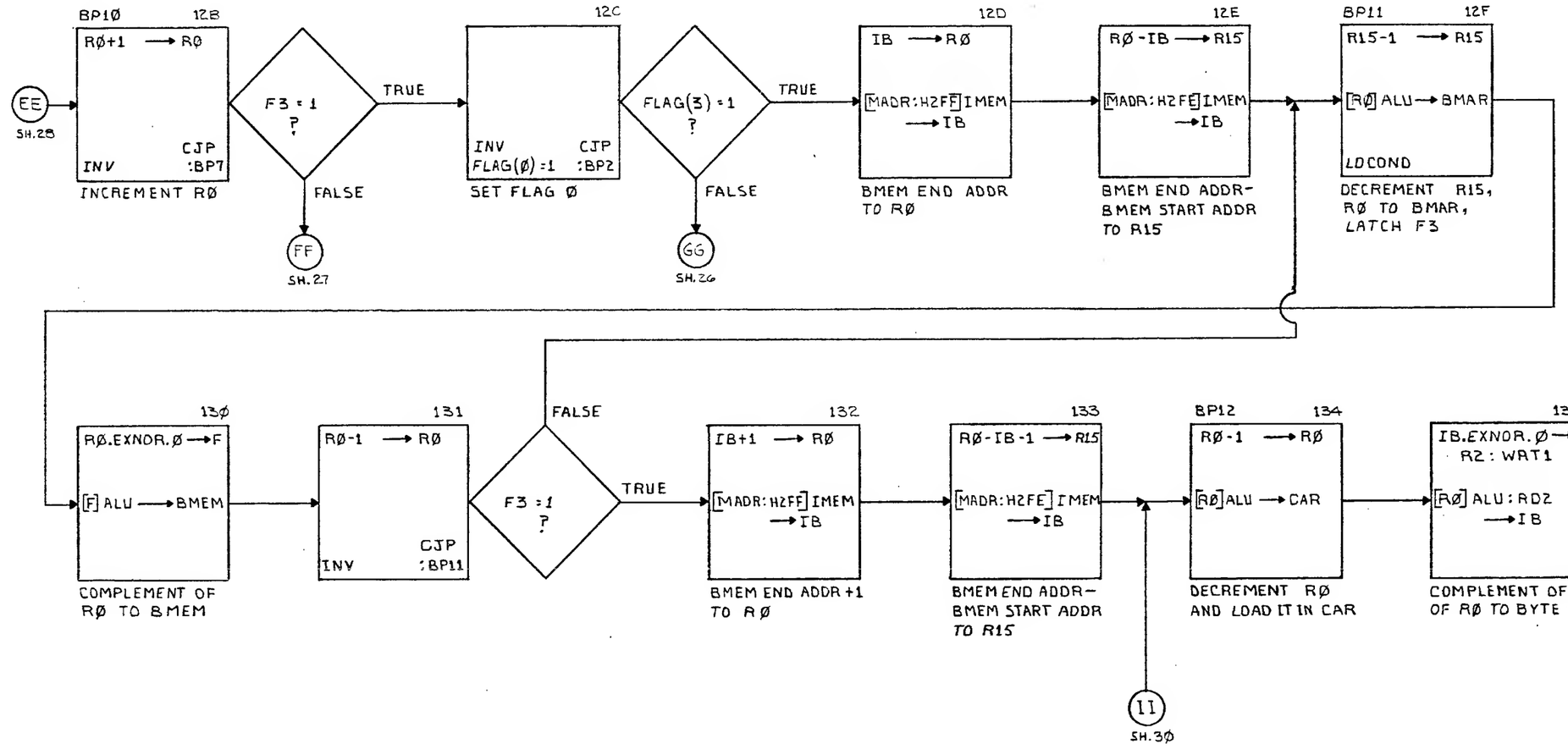
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE * DWG NO. DS21E1065
UNIT WT. * SHEET 28 OF 30 SHEETS

MAKEPEACE P-3059



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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL: X
FINISH: X

PART NUMBER | NEXT ASSEMBLY | QTY

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CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: GPU MICROPROGRAM FLOW CHARTS

SCALE: X
DWG NO. DS21E1065
UNIT WT. X
SHEET 29 OF 30 SHEETS

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DS21E1065
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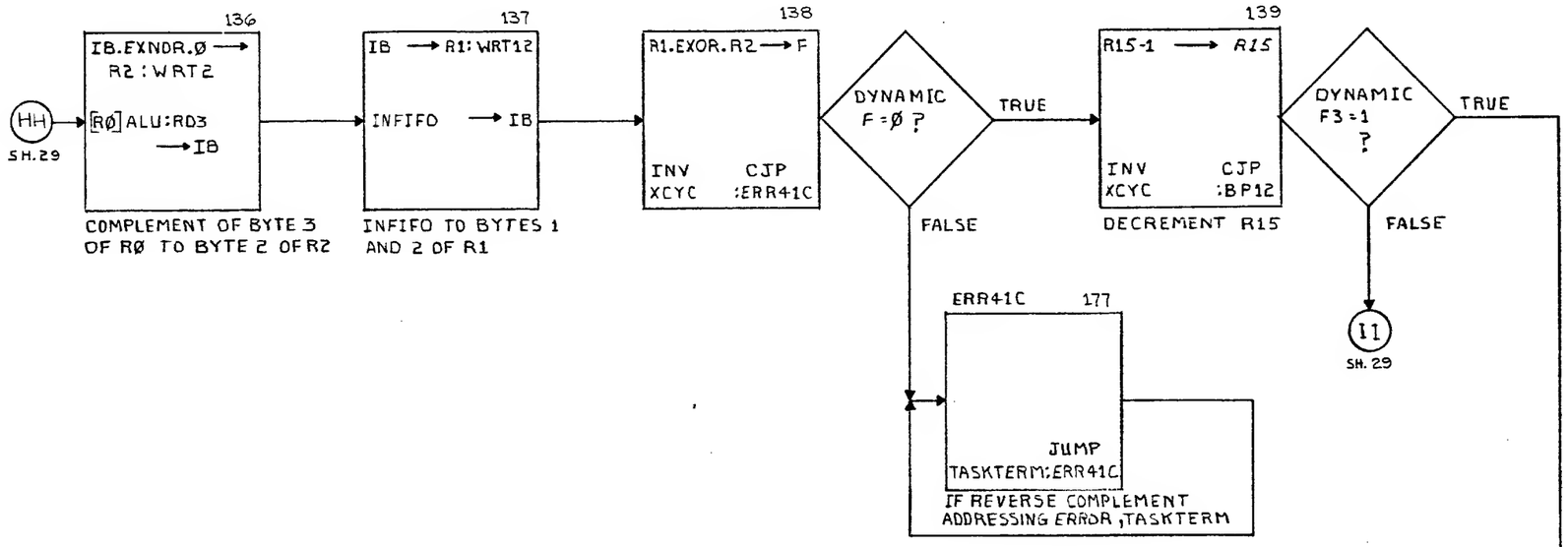

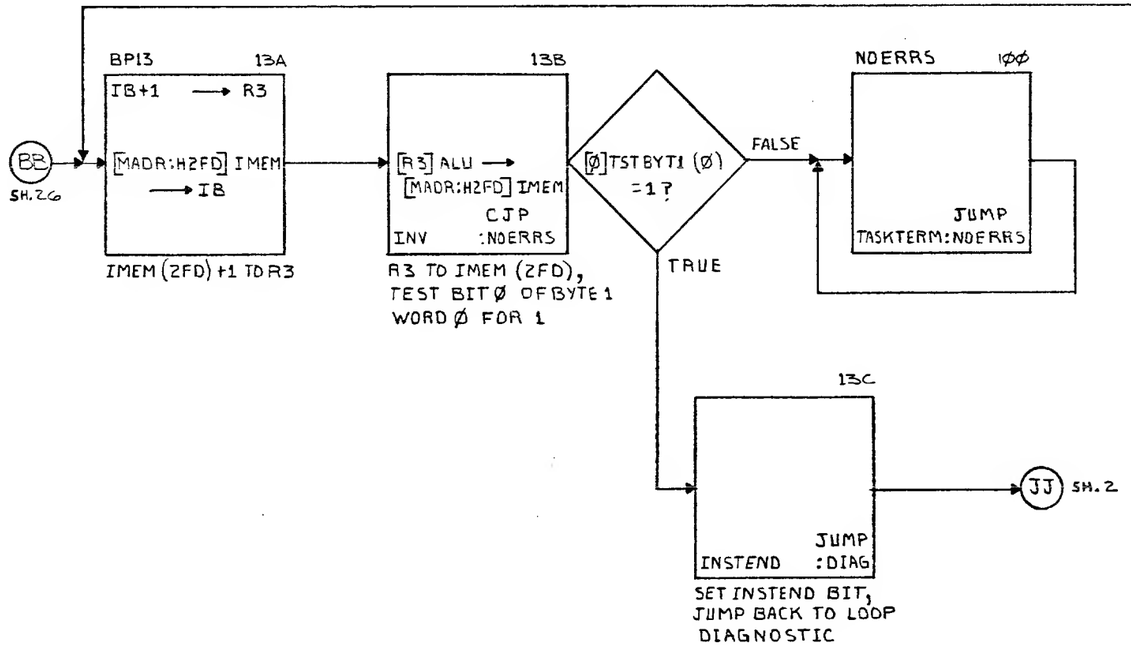

FINISH B PORT TEST, CHECK FOR LOOPING THE DIAGNOSTIC

DS21E1065
B

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MATERIAL x
FINISH x
PART NUMBER | NEXT ASSEMBLY | QTY

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TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN D. O'Hearn 10-79
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PROJ
MFG
SIGNATURE DATE

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE GPU MICROPROGRAM FLOW CHARTS

SCALE x
DWG NO. DS21E1065
UNIT WT. x
SHEET 30 OF 30 SHEETS

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